Performance of the ATLAS Tile Calorimeter in Run 2 and Electronics Upgrade for High Luminosity LHC

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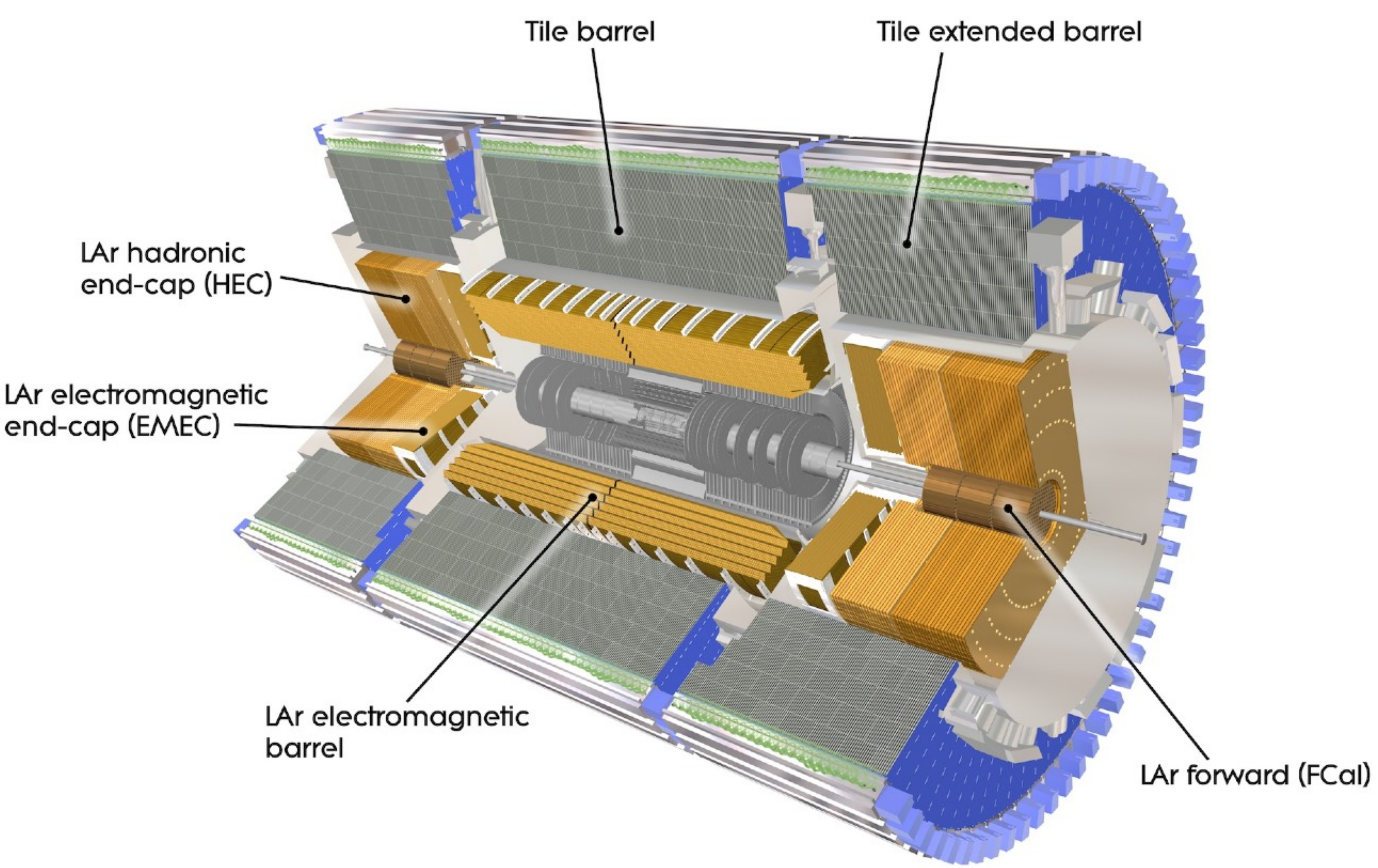
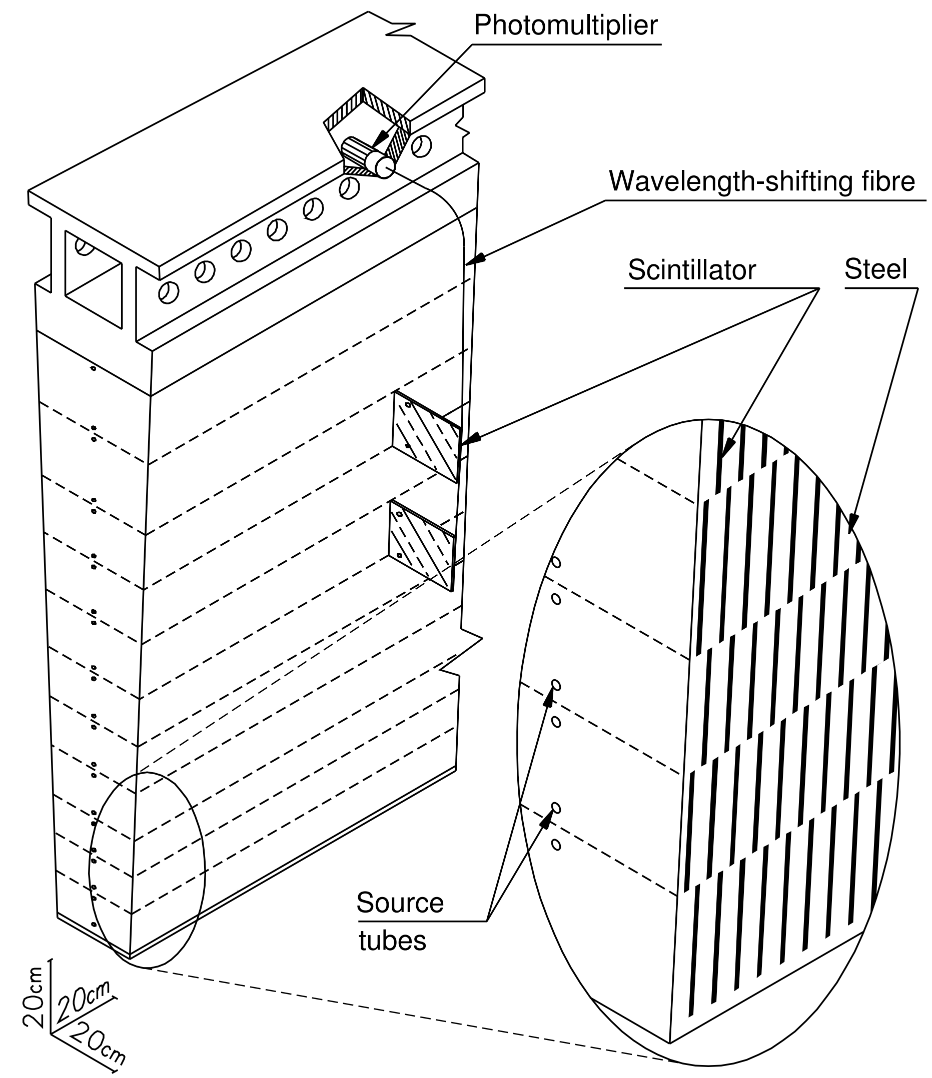
ATLAS EXPERIMENT

THE UNIVERSITY OF CHICAGO

The ATLAS Hadronic Tile Calorimeter (TileCal)

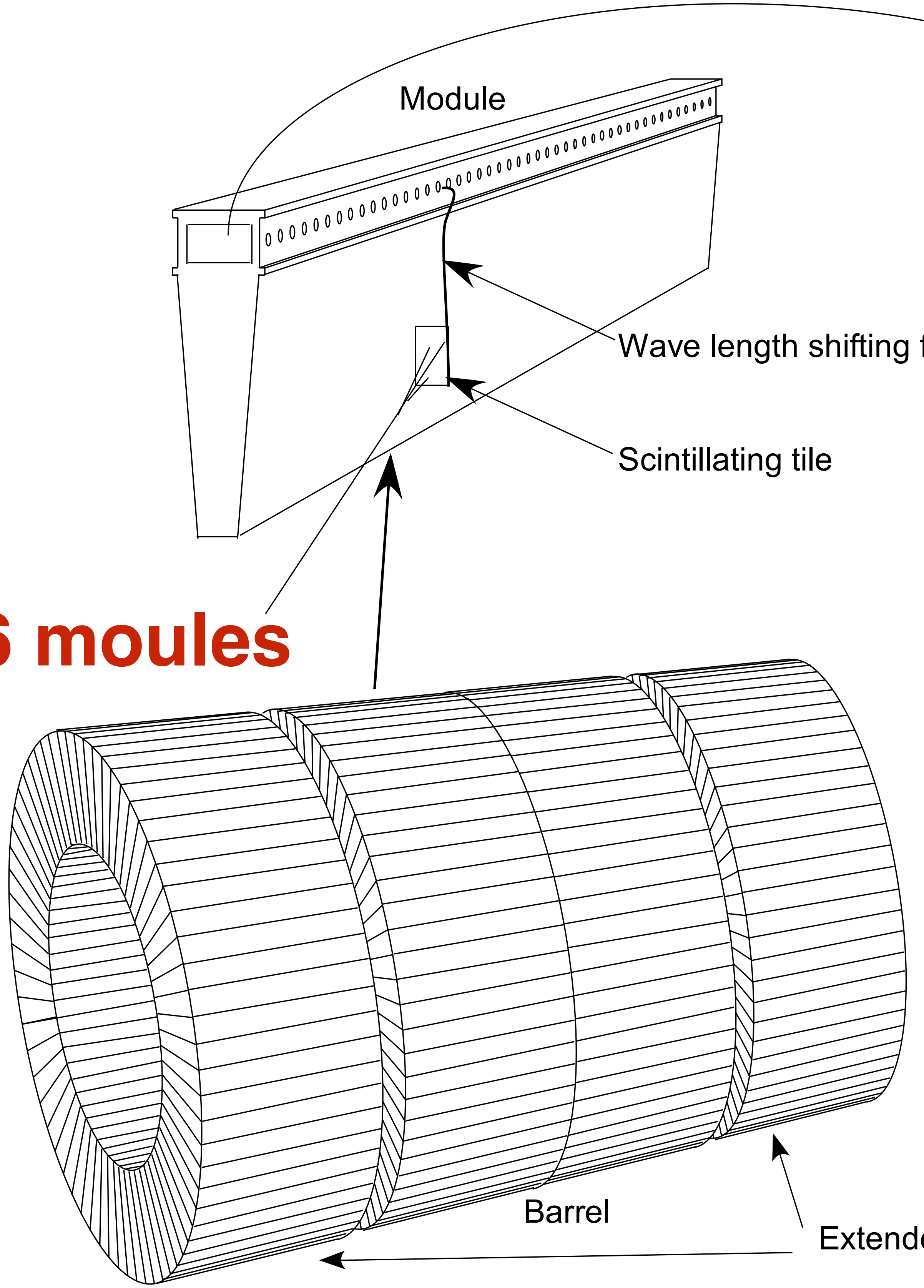
- Hadronic non-compensating sampling calorimeter
  - Composed of steel absorbers and ~500,000 scintillating tiles
  - Read out via fibers coupled to ~10,000 photo-multiplier tubes (PMTs)
  - 2 PMTs per cell ~ 5000 cells
- TileCal (together with the LAr EM calorimeter) is crucial for measuring energy and direction of hadrons



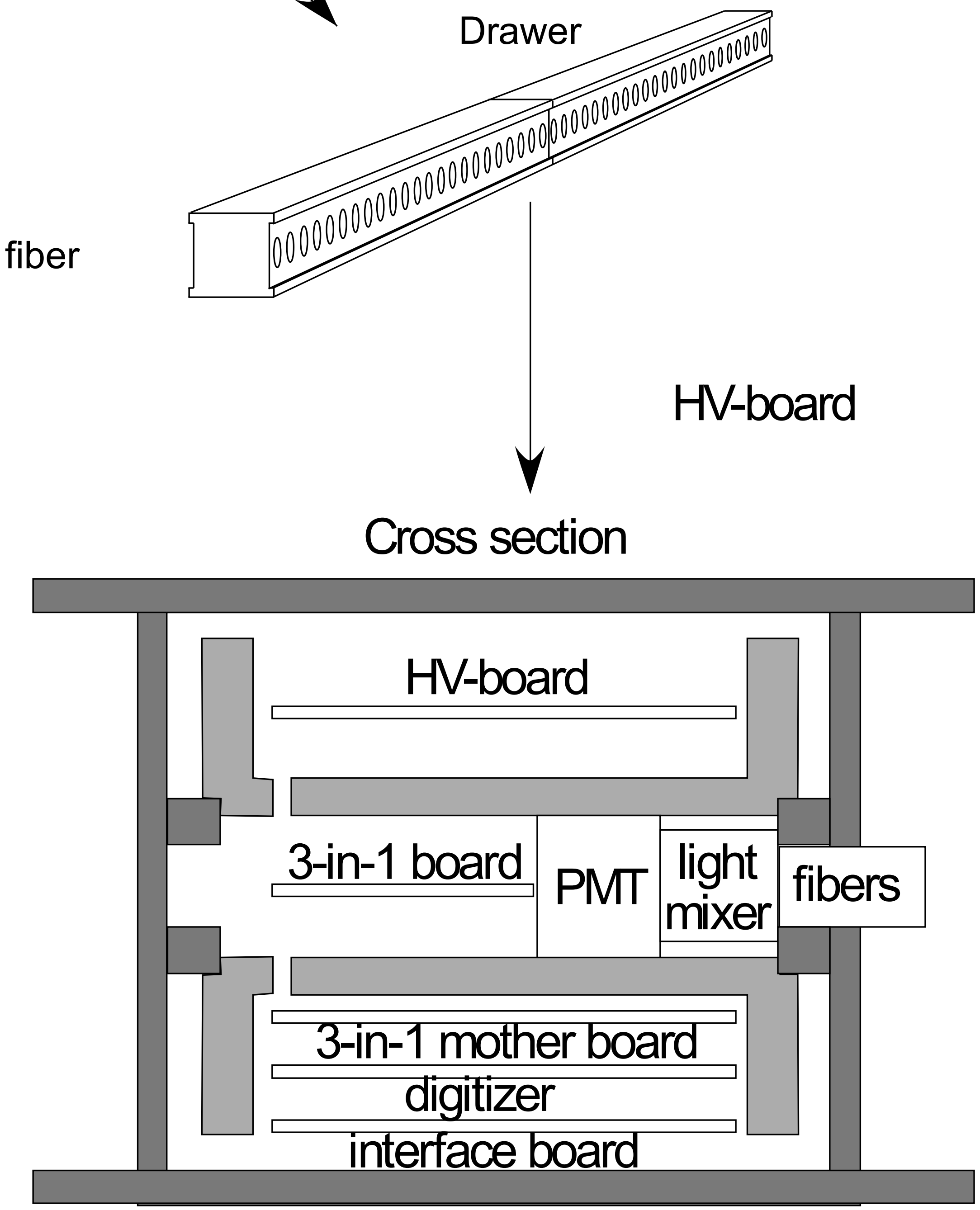


ATLAS TileCal mechanical structure

Electronics drawers

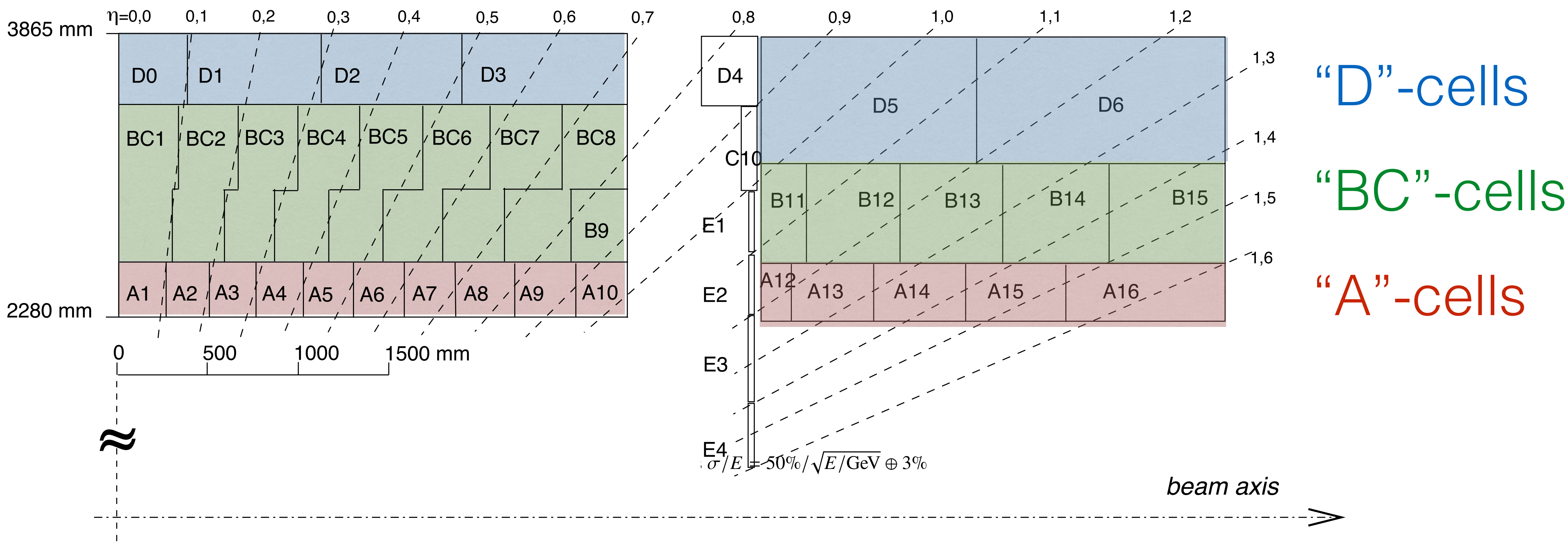


256 moules



Front-end electronics

TileCal cells

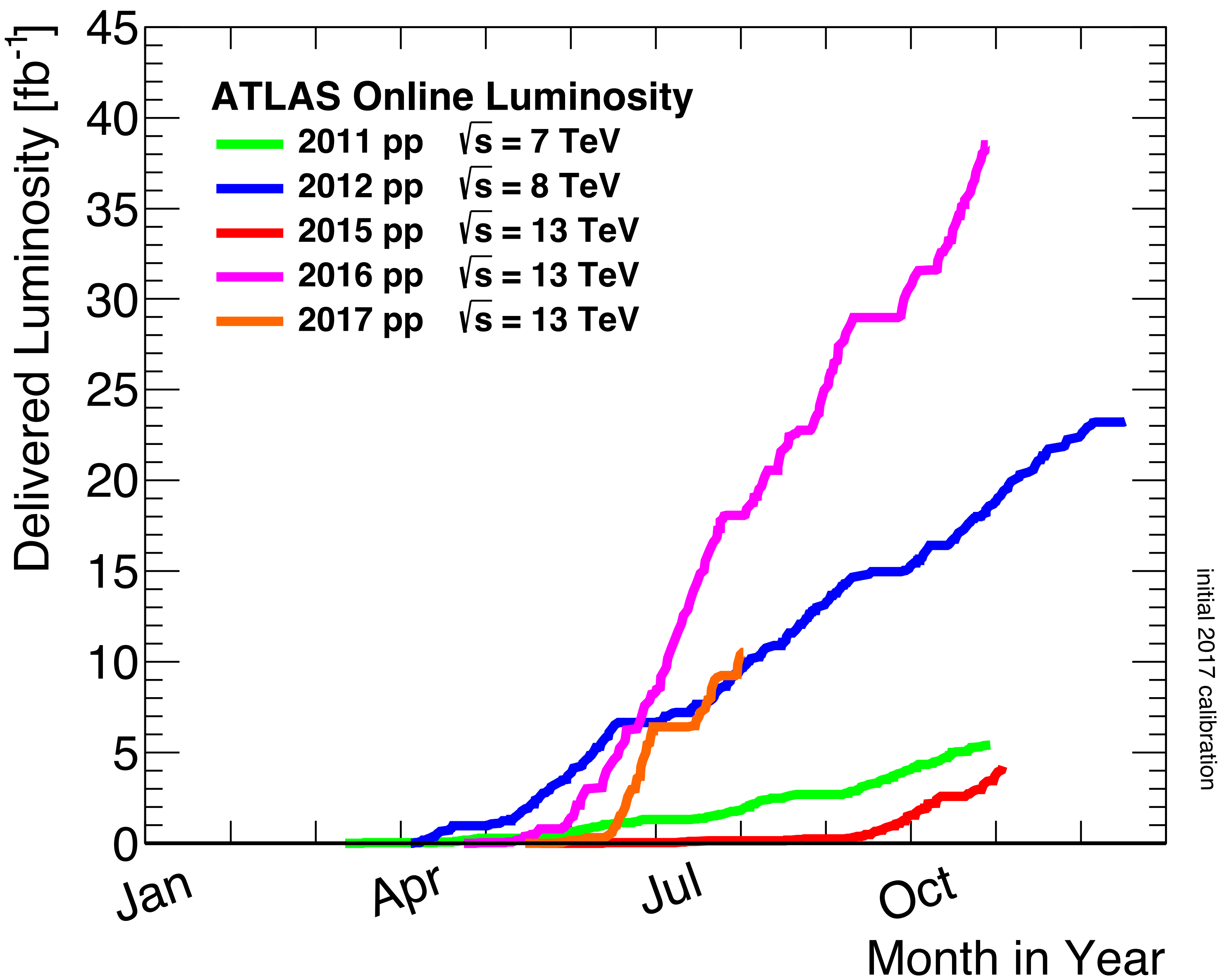


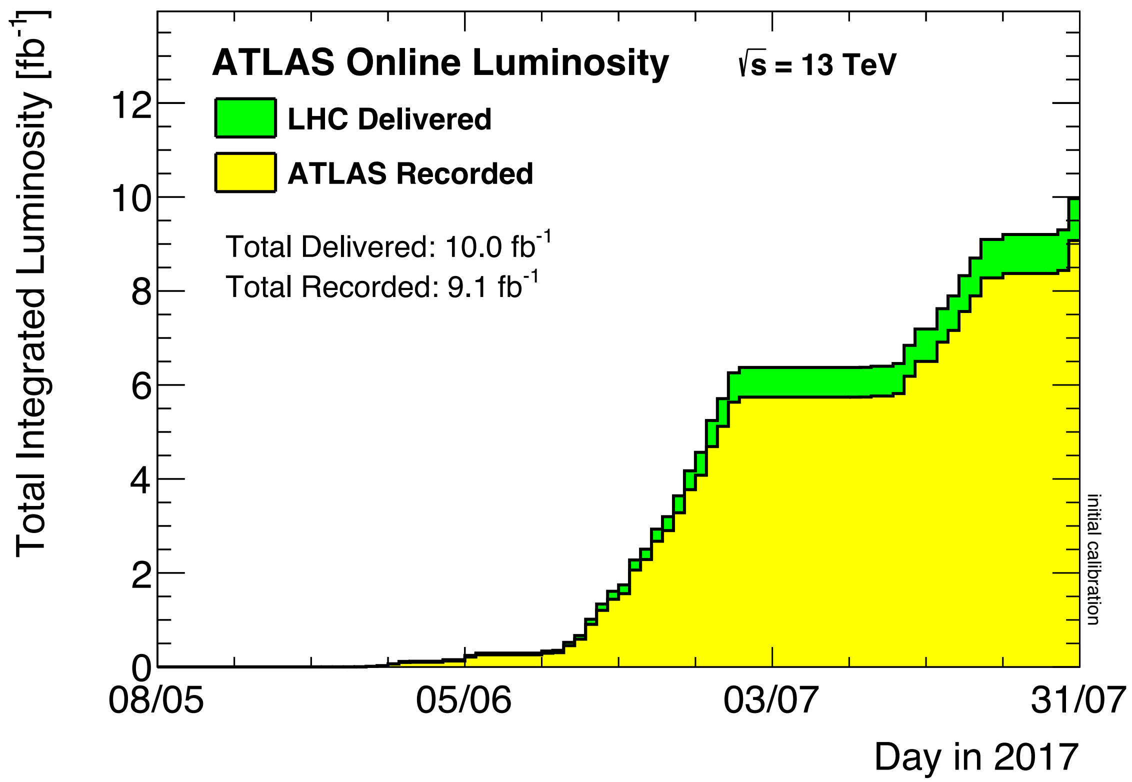
- One long-barrel and two extended barrels
  - Covering |η| < 1.7 and 0 < |ϕ| < 2π
- Three radial layers ($7.4\lambda_{\mathrm{int}}$) for reconstruction of longitudinal showers
- Granularity: |η| x |φ| = 0.1 x 0.1 (0.2 x 0.1 in the D-layer)
- Designed resolution: $\sigma/E = \dfrac{50\%}{\sqrt{E/\mathrm{GeV}}} \oplus 3\%$

Performance of TileCal @ 13 TeV

Excellent performance of the LHC and ATLAS

Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResultsRun2

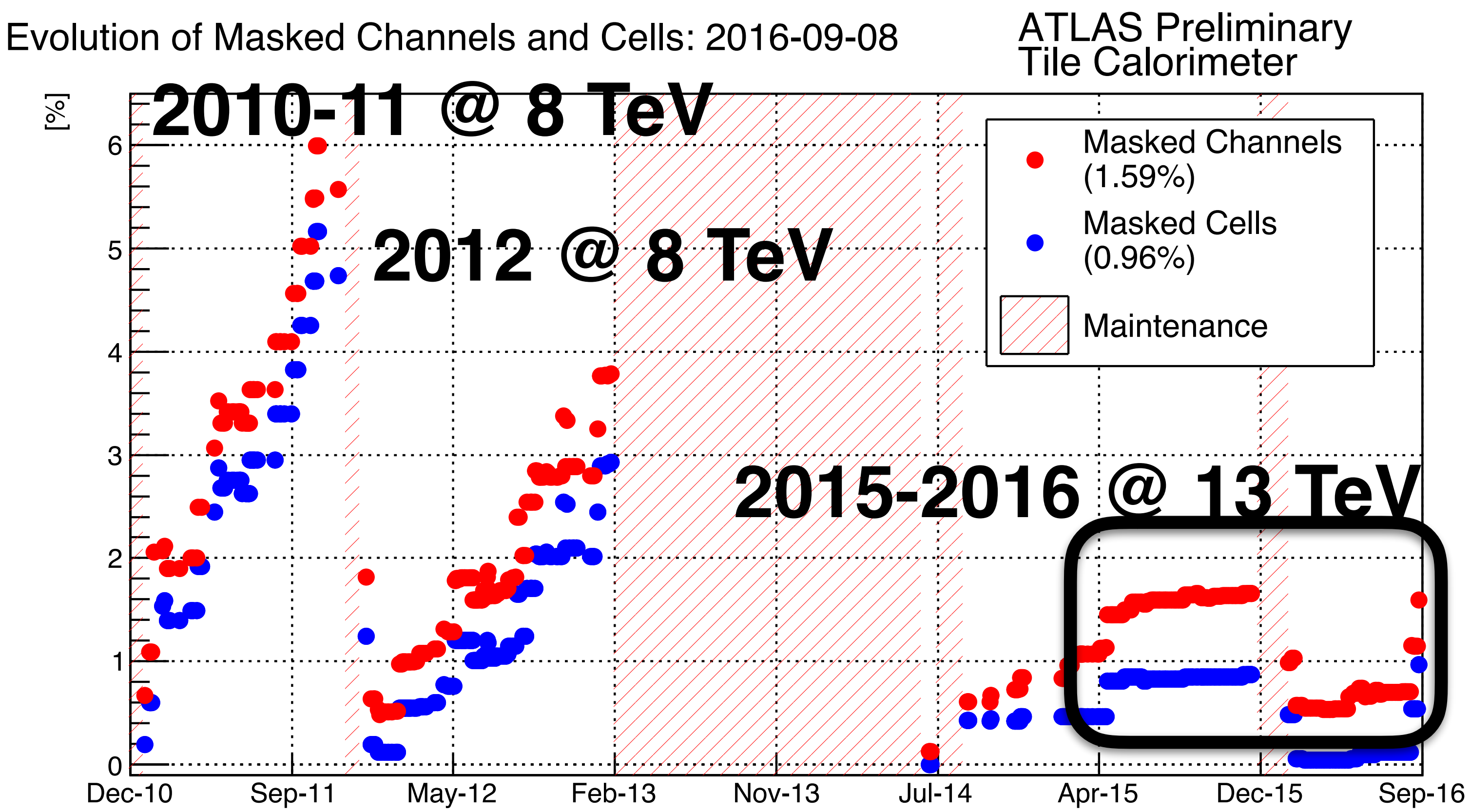


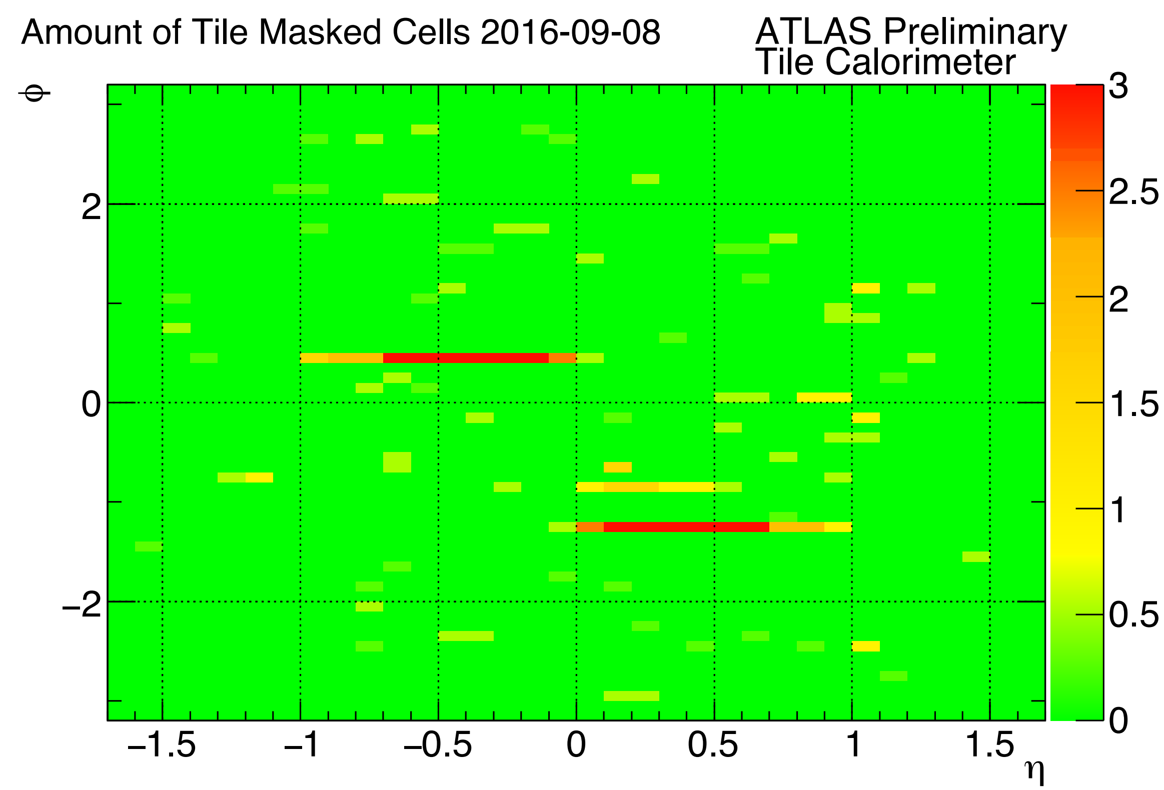


	ATLAS Recored Luminosity
2015	3.9 fb^{-1}
2016	35.6 fb^{-1}
2017 (so far)	10.1 fb^{-1}
Total	**49.6 fb^{-1}**

Percentage of masked cells and channels

Source: 2017 JINST 12 C06021

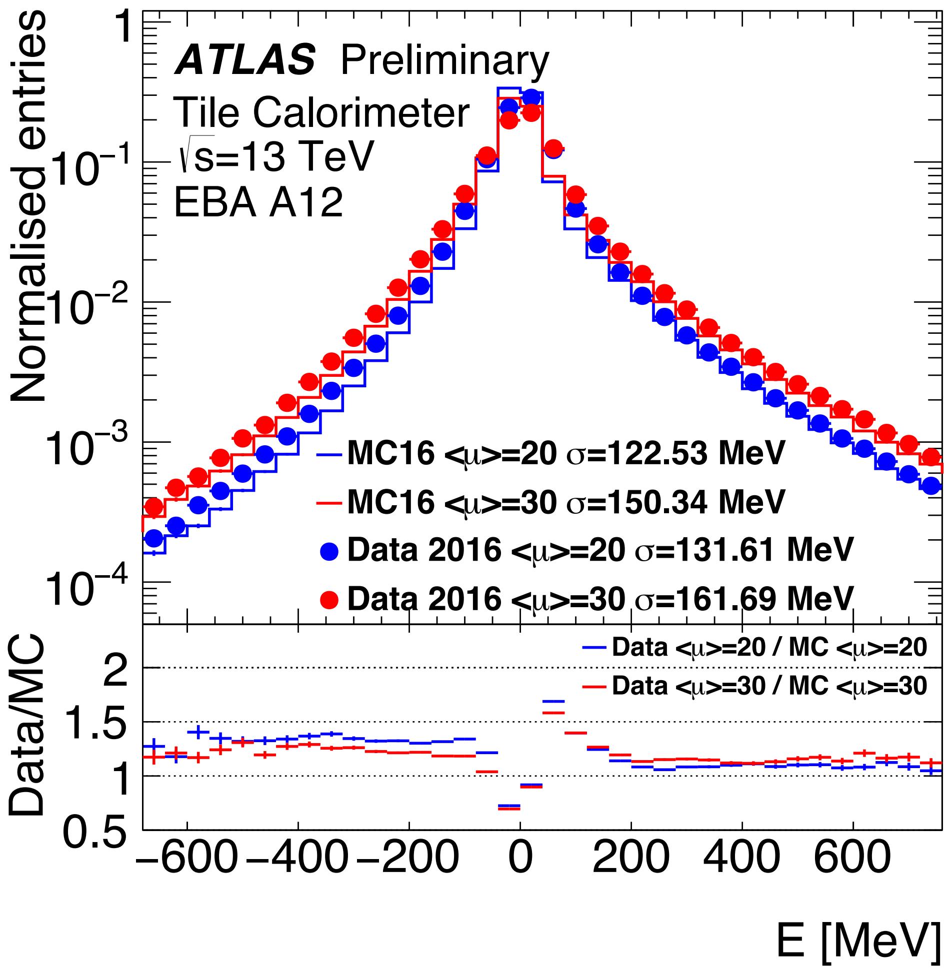


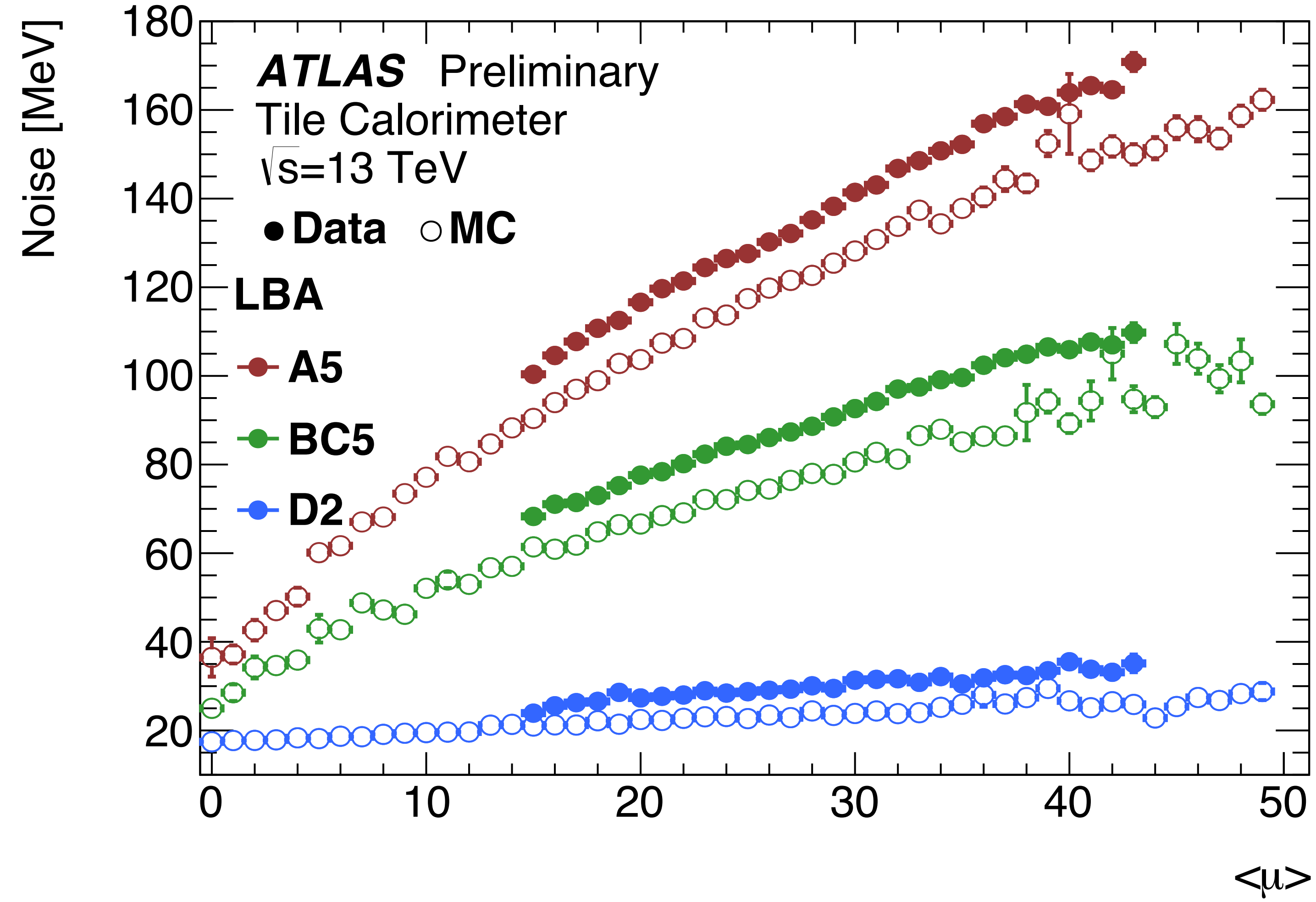


- Cells or channels (TileCal has 2 channels per cell for redundancy) with severe problems that can affect physics data quality are masked to be excluded from physics analysis
- TileCal show **best performance in 2016 with < 1 % of cells masked** at the end of the collision period
  - The 1% of masked cells in 2016 were mostly due to two problematic modules
  - The large number of masked cells in 2011 and 2012 were due to failures in the low voltage power supplies which powers the front-end electronics

Measurement of TileCal noise

Source: 2017 JINST 12 C06021



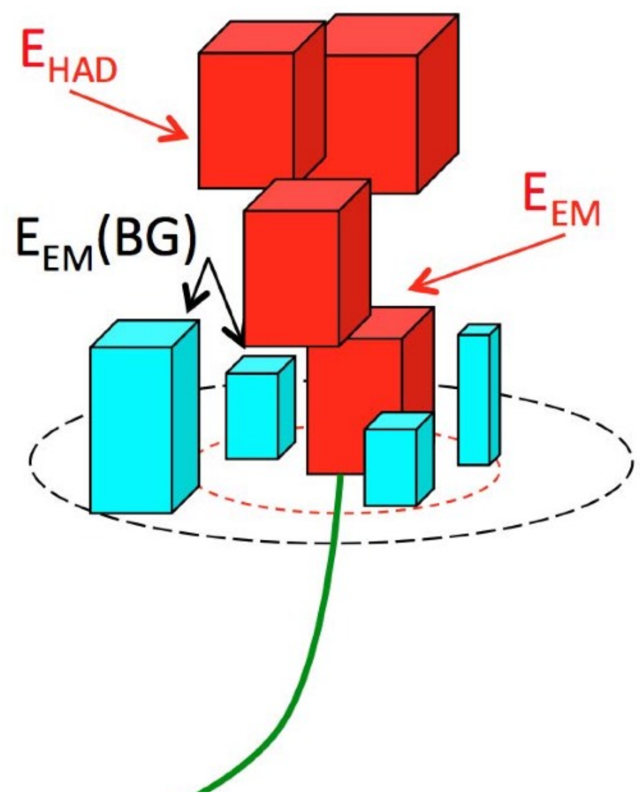


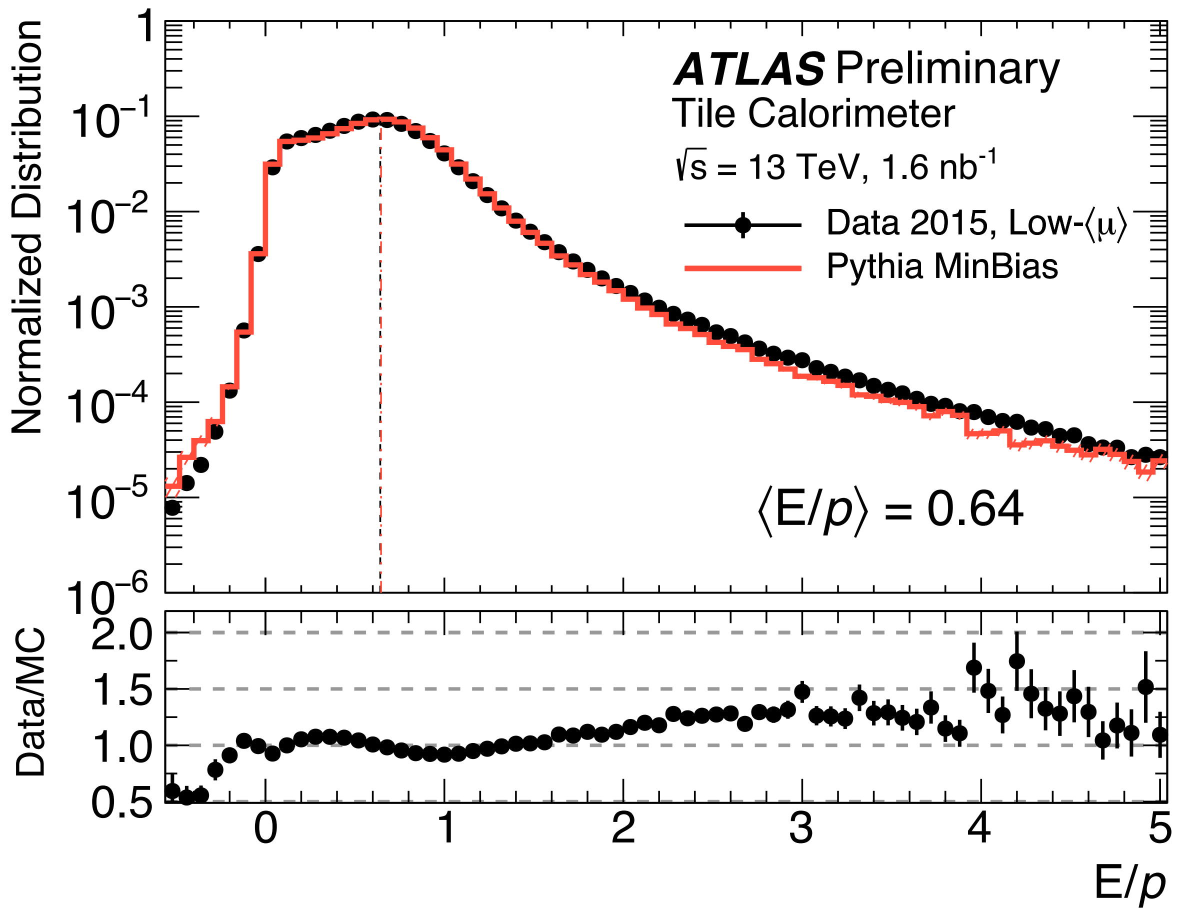
- Noise measurements are essential for the energy reconstruction of physics objects
- Two components: electronics and pile-up noise
  - Electronics noise: Gaussian fit to reconstructed cell energy in special runs without collisions
  - Pile-up effects contribute to the widening of the energy distribution
- Pile-up noise increases with <μ>
- Electronics noise is roughly independent of <μ>

TileCal response to single hadrons (E/p)

Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileSingleParticleResponse

$$\frac{E_{\text{cells,clusters}}}{p_{\text{track}}}$$



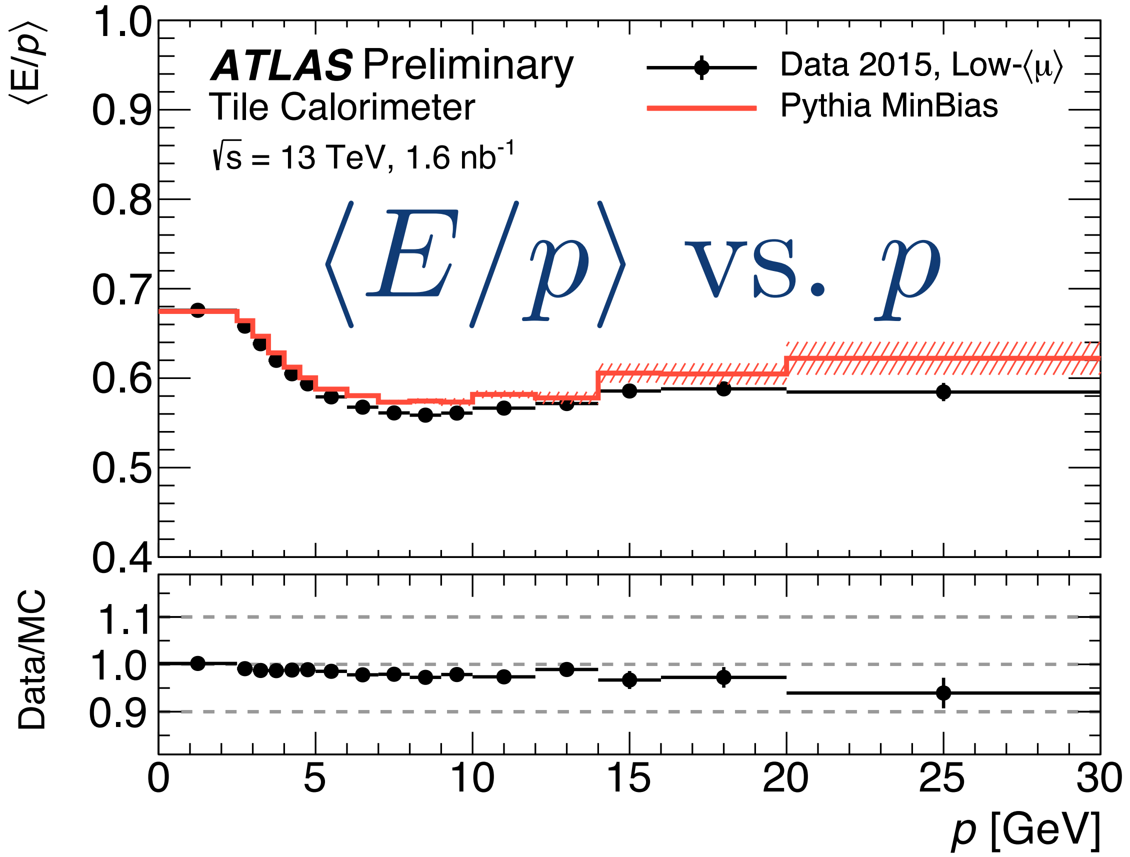


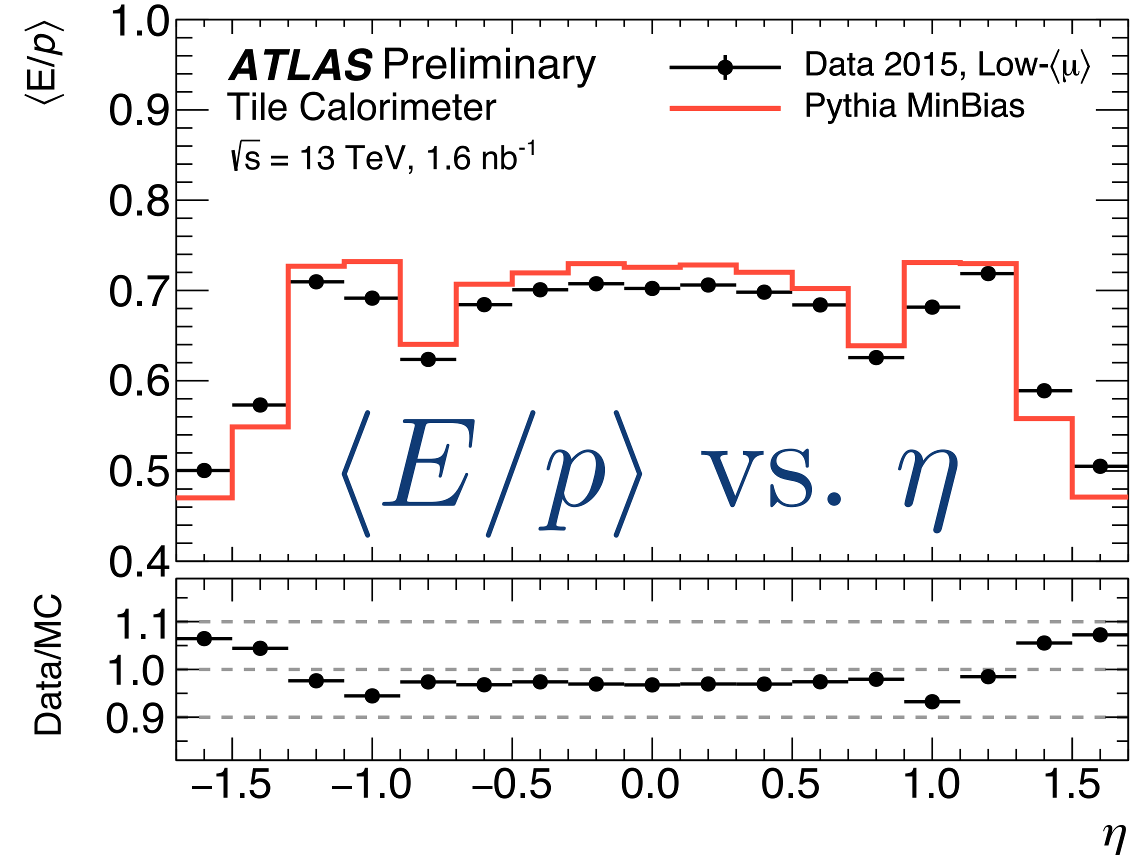
- What is E/p?
  - Momentum from isolated charged hadrons (tracks) from the inner detector
  - Extrapolate tracks to the calorimeter and sum energy in a cone to form E/p
  - E/p < 1 due to sampling and non-compensating nature of calorimeter
- Why E/p?
  - Validation of hadronic shower modeling and detector geometry
  - **Important input to jet energy scale (JES) uncertainty**

Measured average E/p response in TileCal

Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileSingleParticleResponse

Low (~1) number of pp collisions per bunch crossing





- Selections to reject background
  - **Charged hadrons:** No other tracks allowed within a cone of $\Delta R < 0.4$ of selected track
  - **Neutral hadrons:** Energy in EM calo compatible with minimum ionizing particle
  - **Muons:** Require a 70% of the energy to be deposited in TileCal
- Good agreement between Data and MC

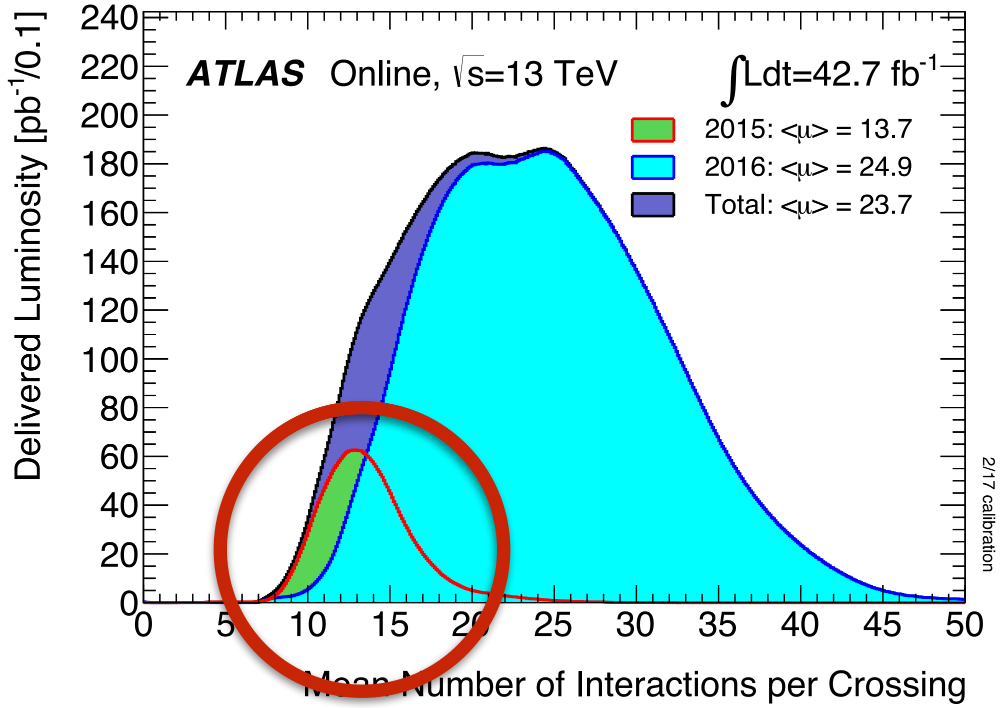
Measured average E/p response in TileCal

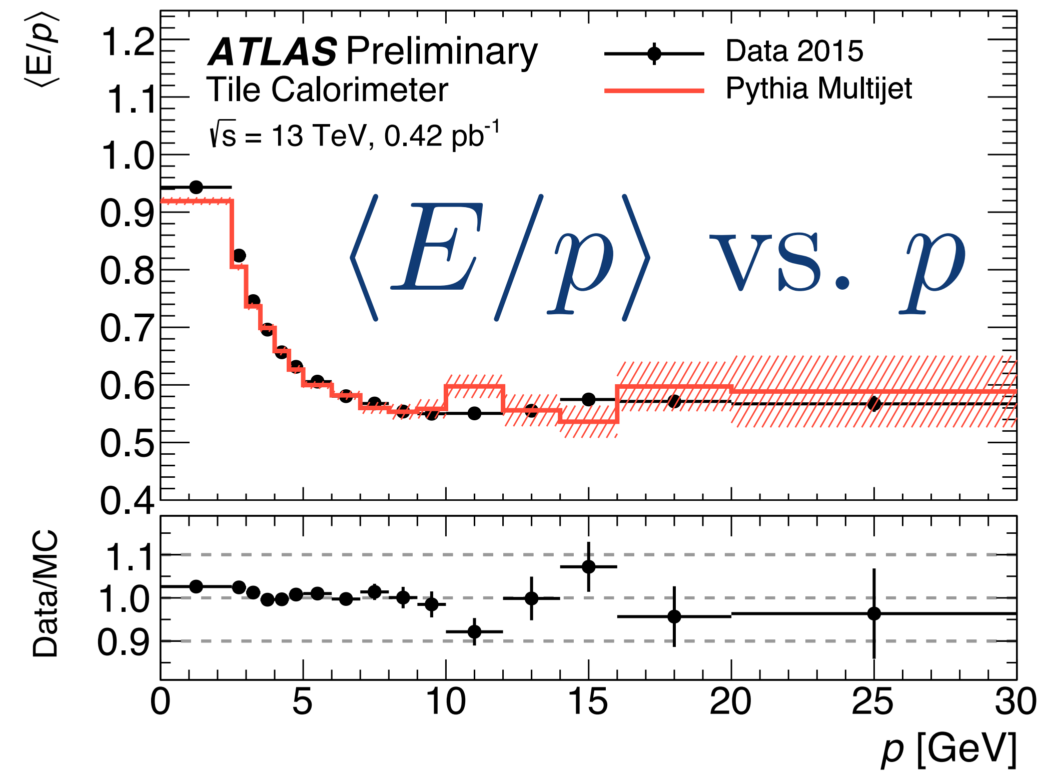
Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileSingleParticleResponse

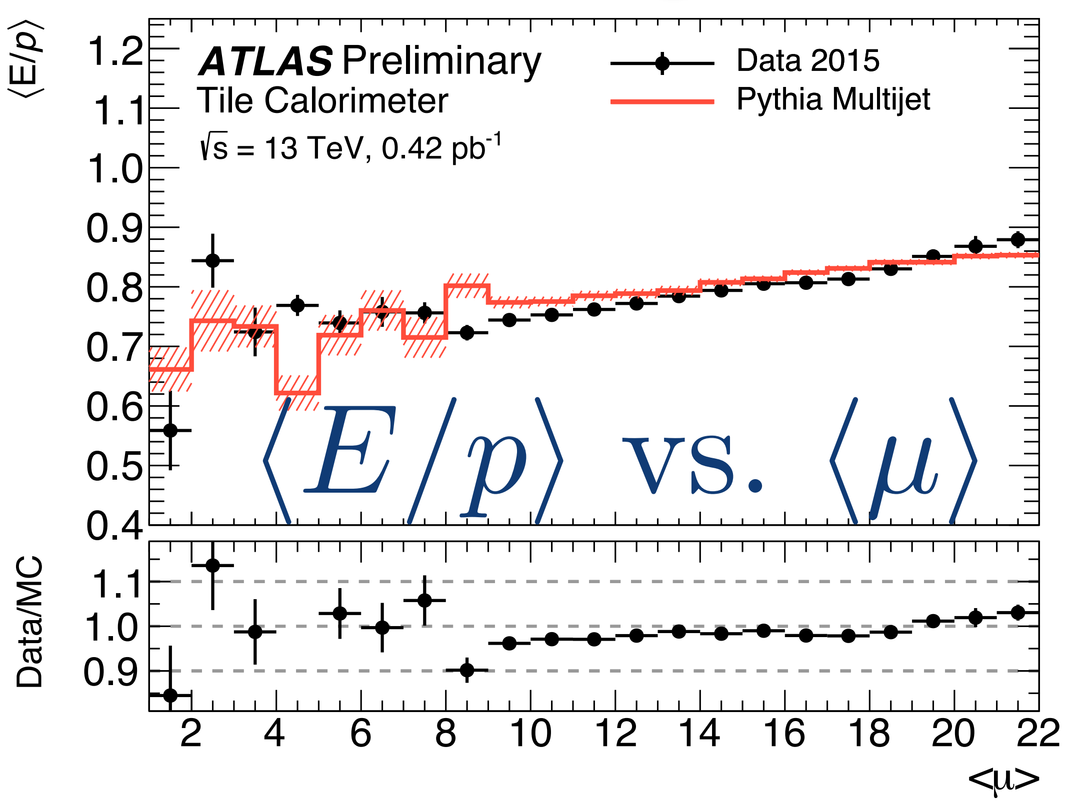
Multiple pp collisions per bunch crossing (pile-up)

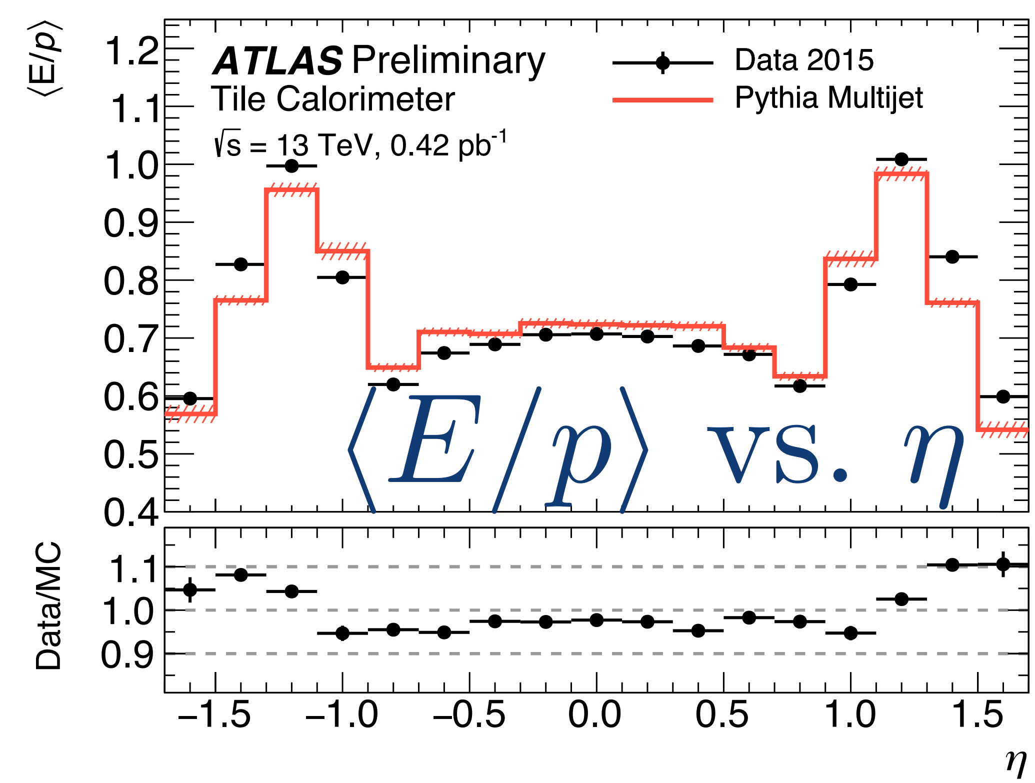
2015:

$\langle \mu \rangle = 13.7$










Readout electronics upgrade for High-Luminosity LHC

Motivation for upgrade

HL-LHC

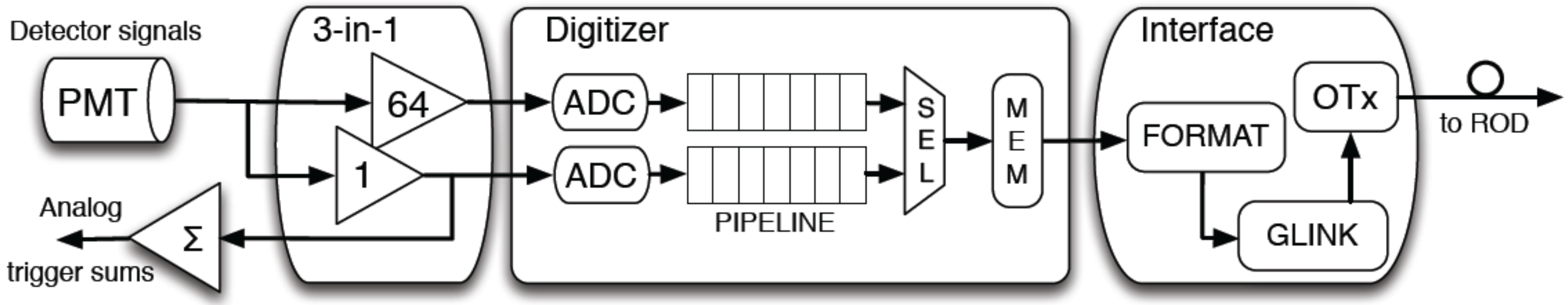
2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028+
← Run 2 →				← LS2 →		← Run 3 →			← LS3 →			← Run 4 + →	

- High-Luminosity LHC (HL-LHC) ~ mid 2026
  - Extend the discovery potential and take full advantage of the LHC
  - 10x the integrated luminosity (4000 fb^{-1}) of LHC runs 1-3, combined
- Detector components do not need to be replaced
  - Steel absorbers, scintillating tiles, and wavelength shifting fibers will survive
  - May need to replace PMTs in high occupancy regions (PMT lifetime studies ongoing)
- Readout electronics must be replaced
  1. Current TileCal readout is not compatible with the planned **fully digital** ATLAS HL-LHC readout and trigger architecture
  2. Degradation (and aging) of electronics due to radiation (and time)
  3. Improved *reliability* through *redundancy* and *simplicity*

The new readout architecture

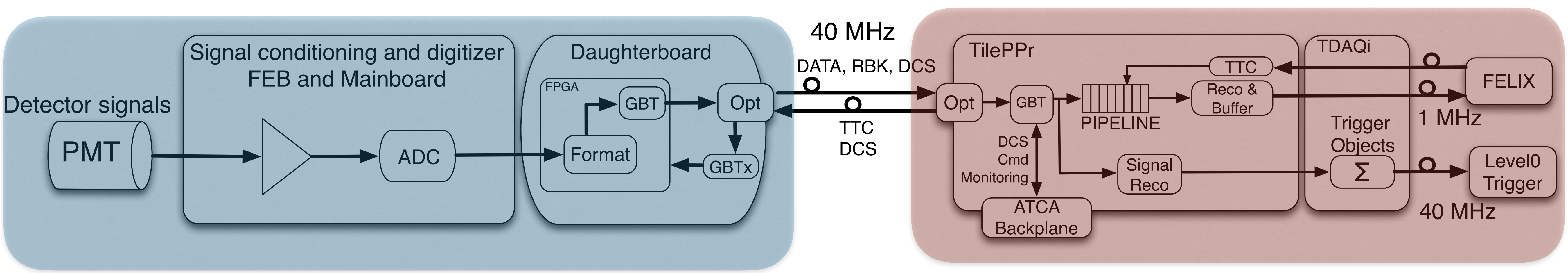
Improved ***reliability*** *through* ***redundancy*** *and* ***simplicity***

Current readout architecture



New readout architecture

Front-end electronics (on-detector) **Back-end electronics (off-detector)**

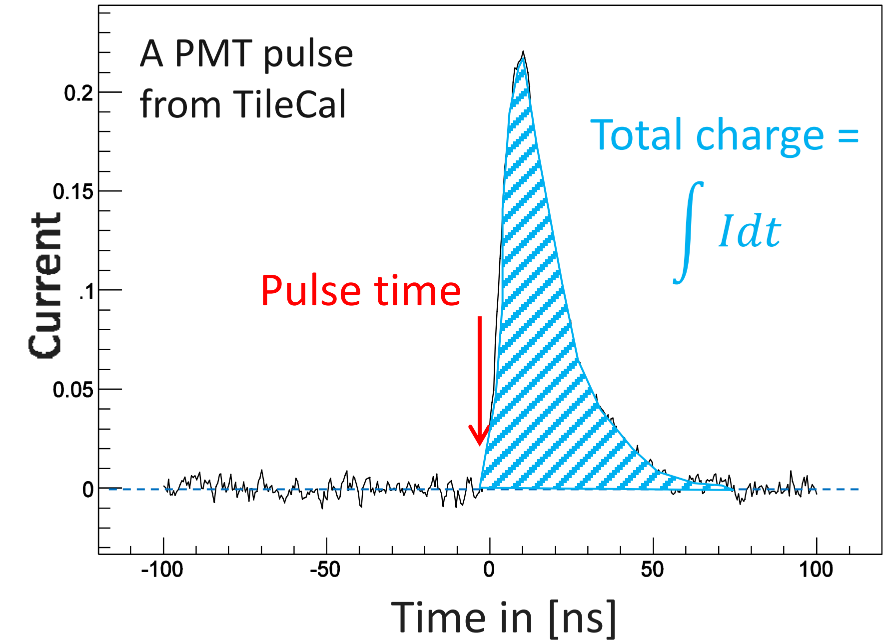


- All digital data is transmitted off-detector at 40 MHz
  - Present system designed to output digital data at the maximum rate of 100 kHz
- The data is pipelined and processed in the off-detector Pre-Processor (PPr)

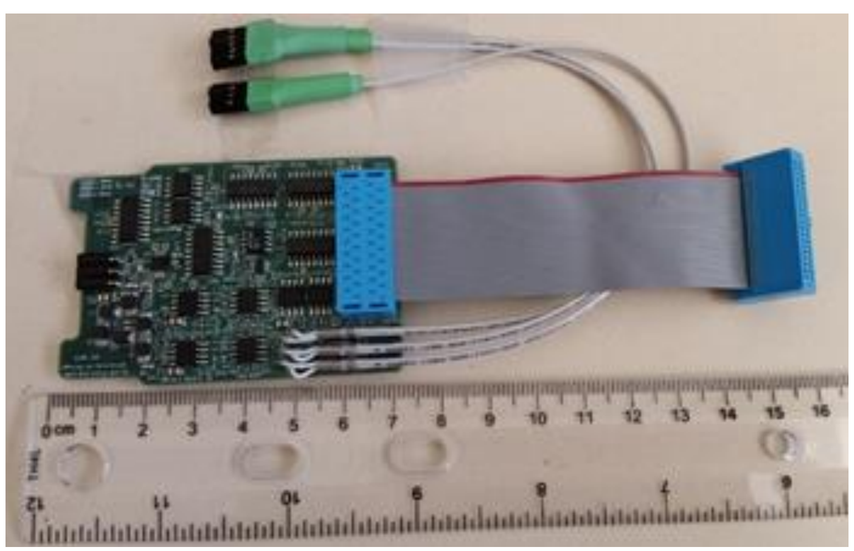
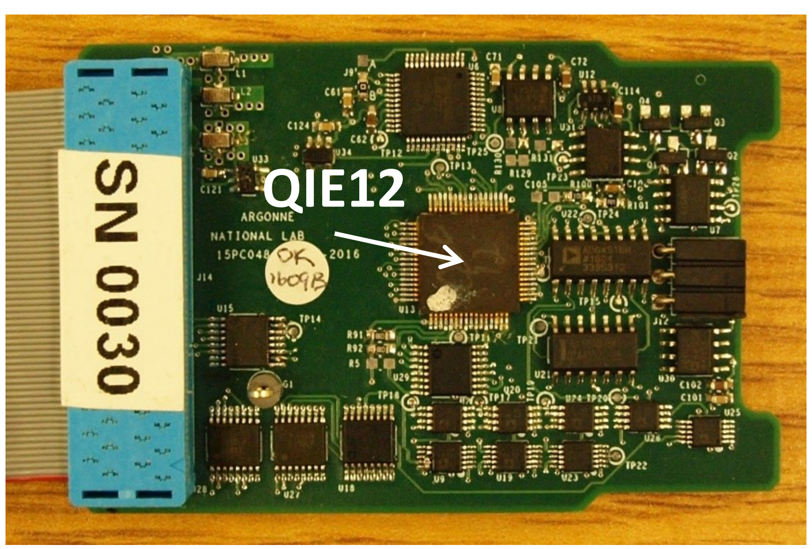
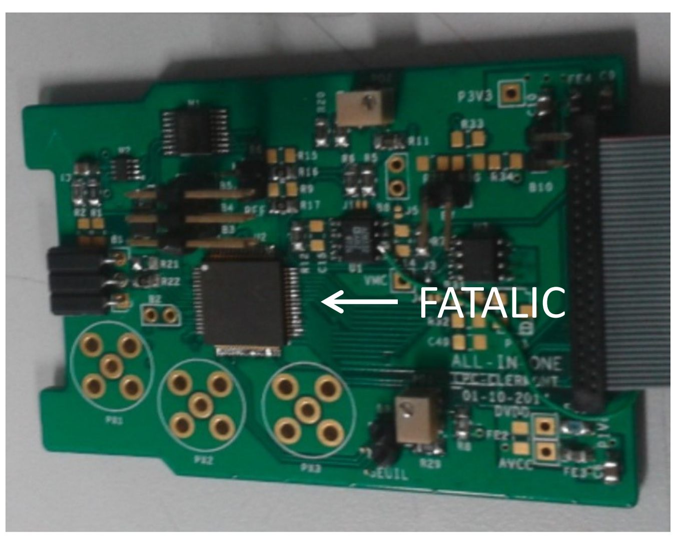
Digitization of the PMT signals

- Need to measure **time** and **total charge** for each PMT pulse
- Challenge: pulses are short and subject to photo-statistical fluctuations
- Digitization of PMT pulse is done by a dedicated front-end board

Image source: A. Paramonov



Three different front-end technologies have been tested

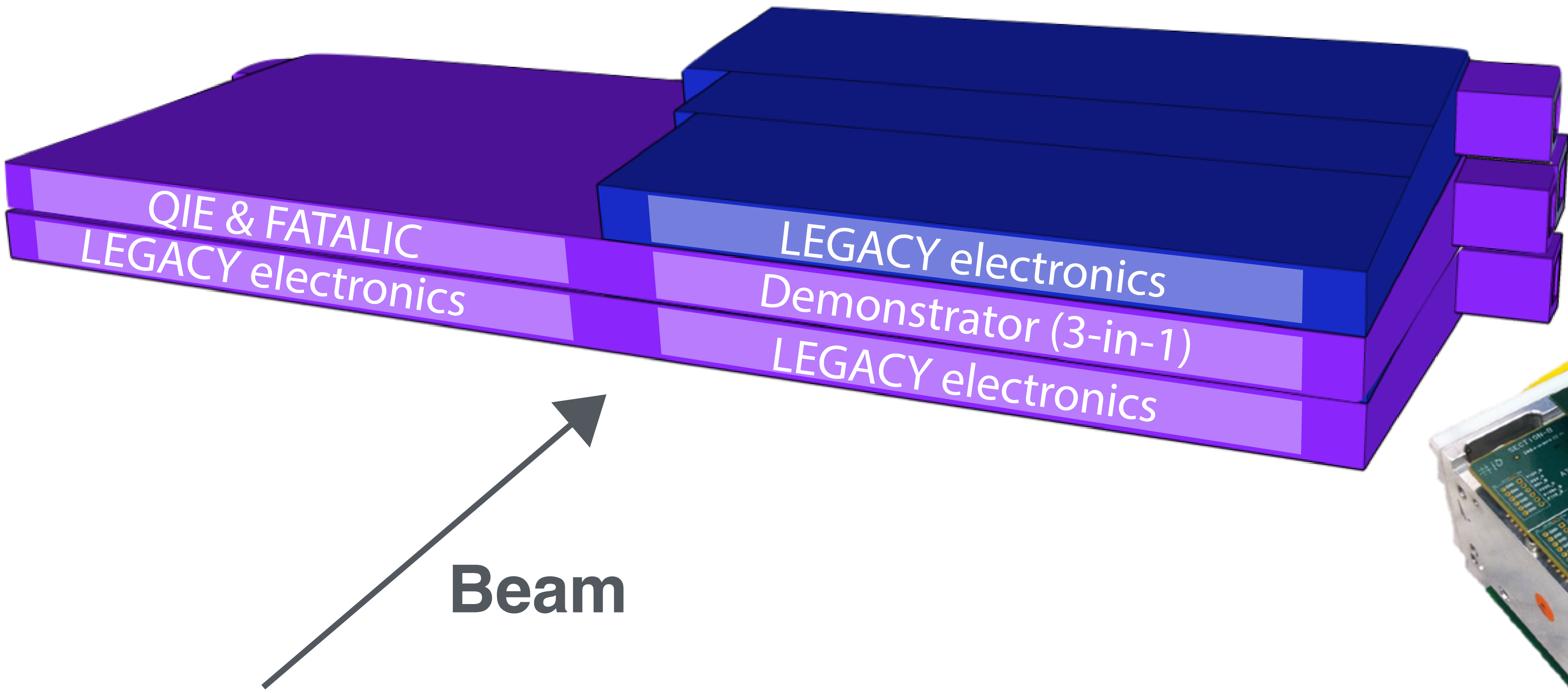
Upgraded "3-in-1" (discrete)	QIE (ASIC)	FATALIC (ASIC)
		
Pulse shaper	Charge integrator	Pulse shaper

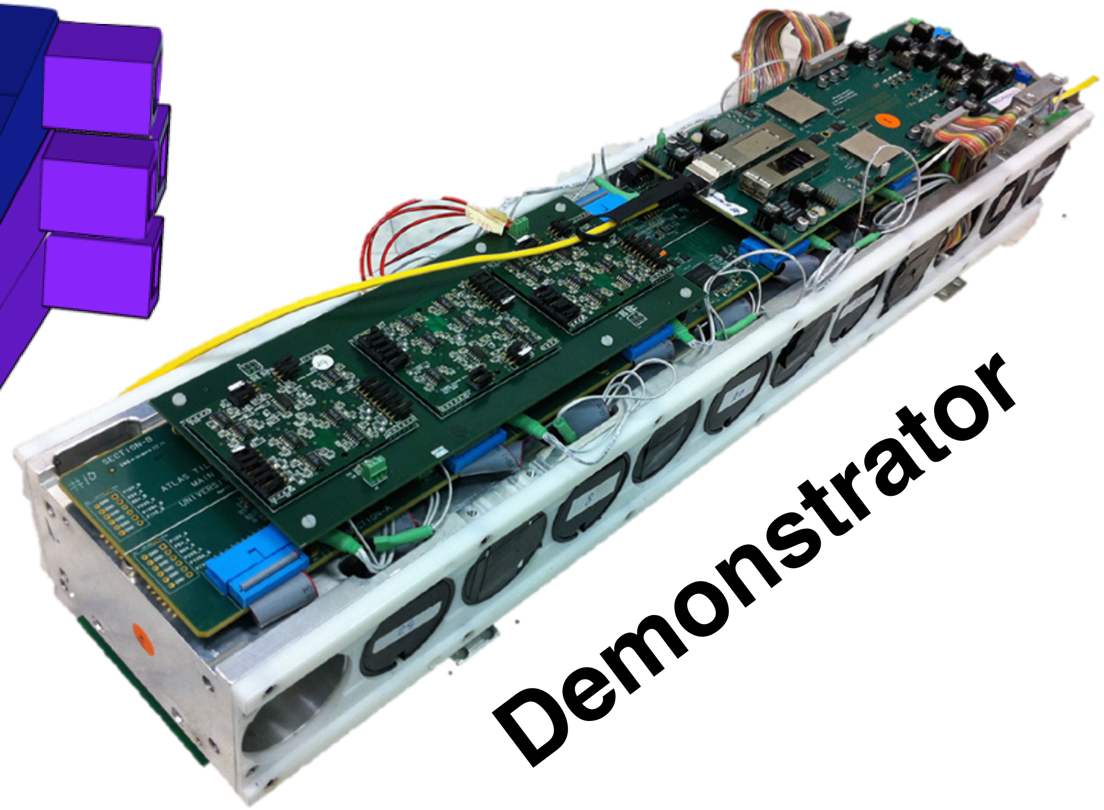
Status of the upgrade electronics

- Front-end (on-detector) electronics
  - Three different front-end technologies have been evaluated; upgraded 3-in-1, QIE, and FATALIC
  - A decision was recently made to proceed with the upgraded 3-in-1
  - Evaluating new version of the high-speed communications board
  - Testing new low voltage power supply (LVPS) — redundant 10V local point of load regulators at the front-end
  - Evaluating two options for HV; remote and local
- Back-end (off-detector) electronics
  - Tile Pre-Processor (TilePPr),Trigger and Data Acquisition interface (TDAQi), and FELIX (readout of the TilePPr) under design and prototyped
  - TilePPr demonstrator already being used in test beams

TileCal test beam program in 2017

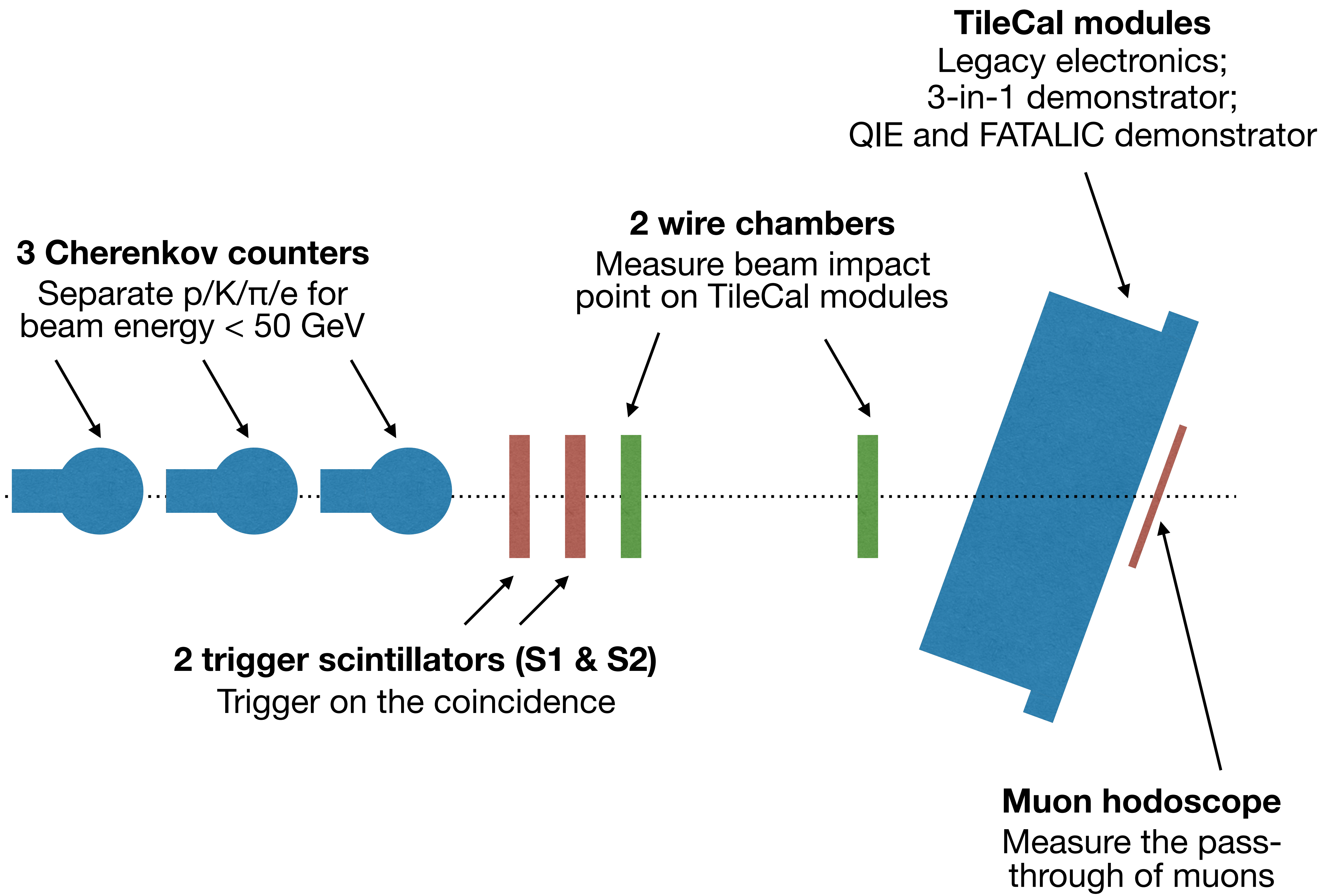
June 16-28 and September 6-20, 2017
Previously in June 2016, September 2016, and October 2015



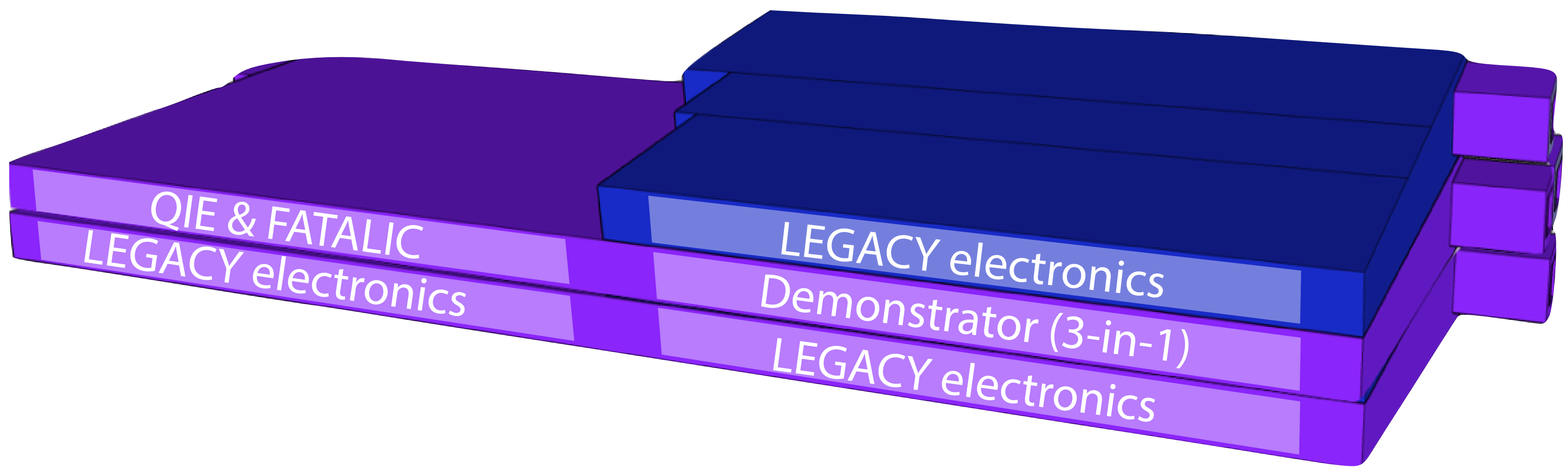


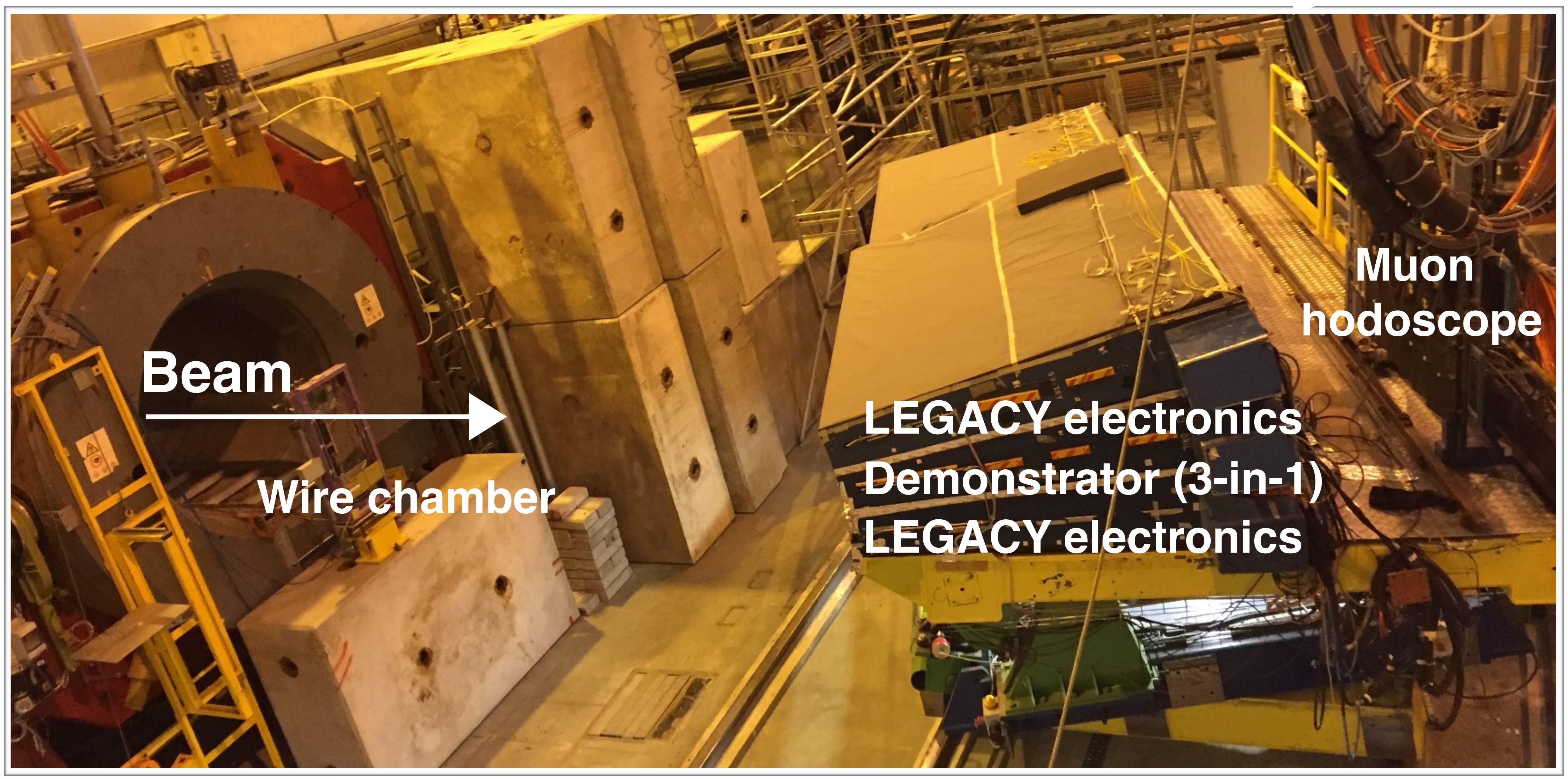
- **Main goal:** validation of the upgrade electronics
  - Test the reliability of the whole system
  - Study the performance of different front-end technologies
  - Test two different systems for HV supply; local and remote
- **Additional goal:** calorimeter measurements of μ, e, $\pi^{\pm}$, $K^{\pm}$

Test beam setup at CERN

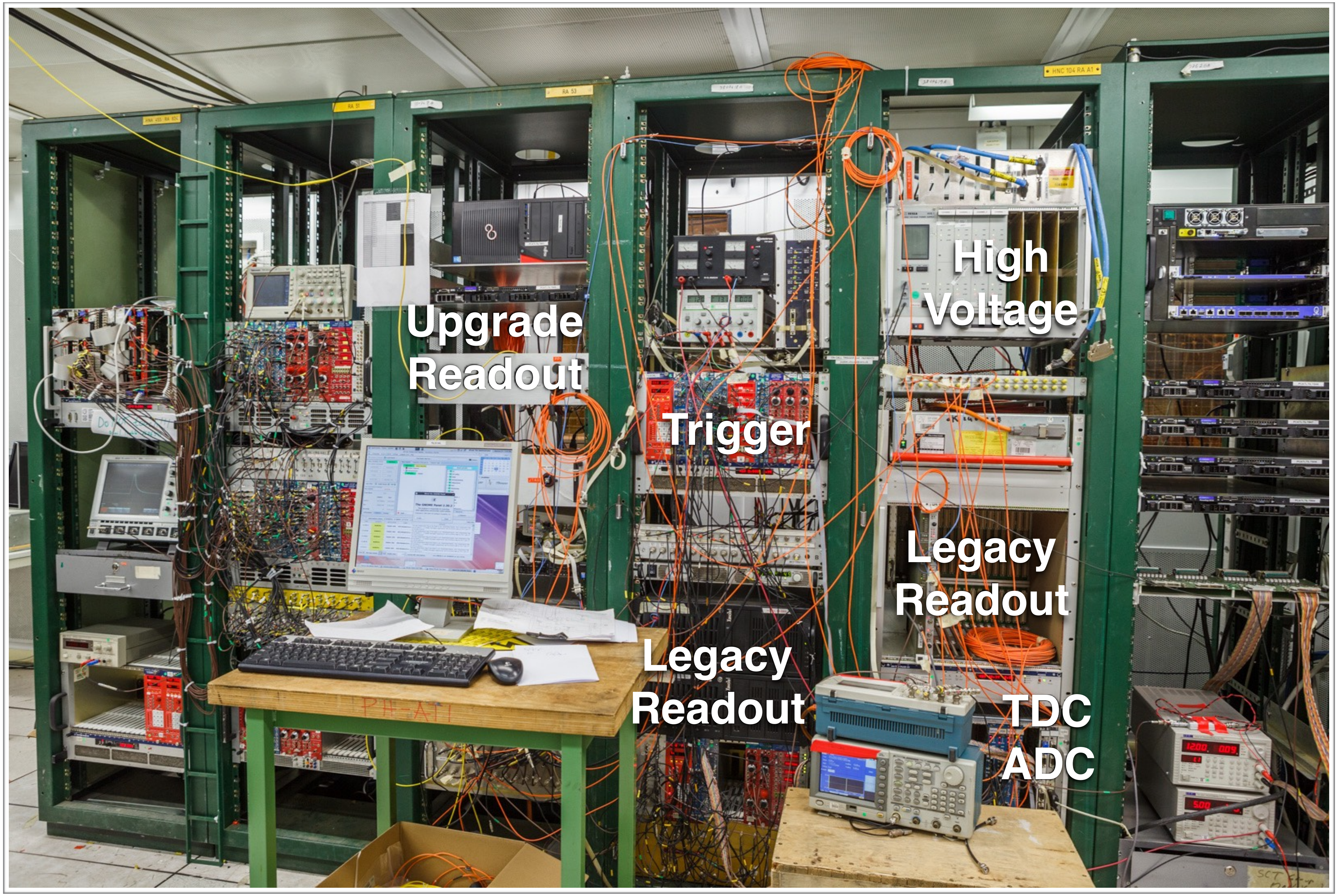


Test beam setup at CERN





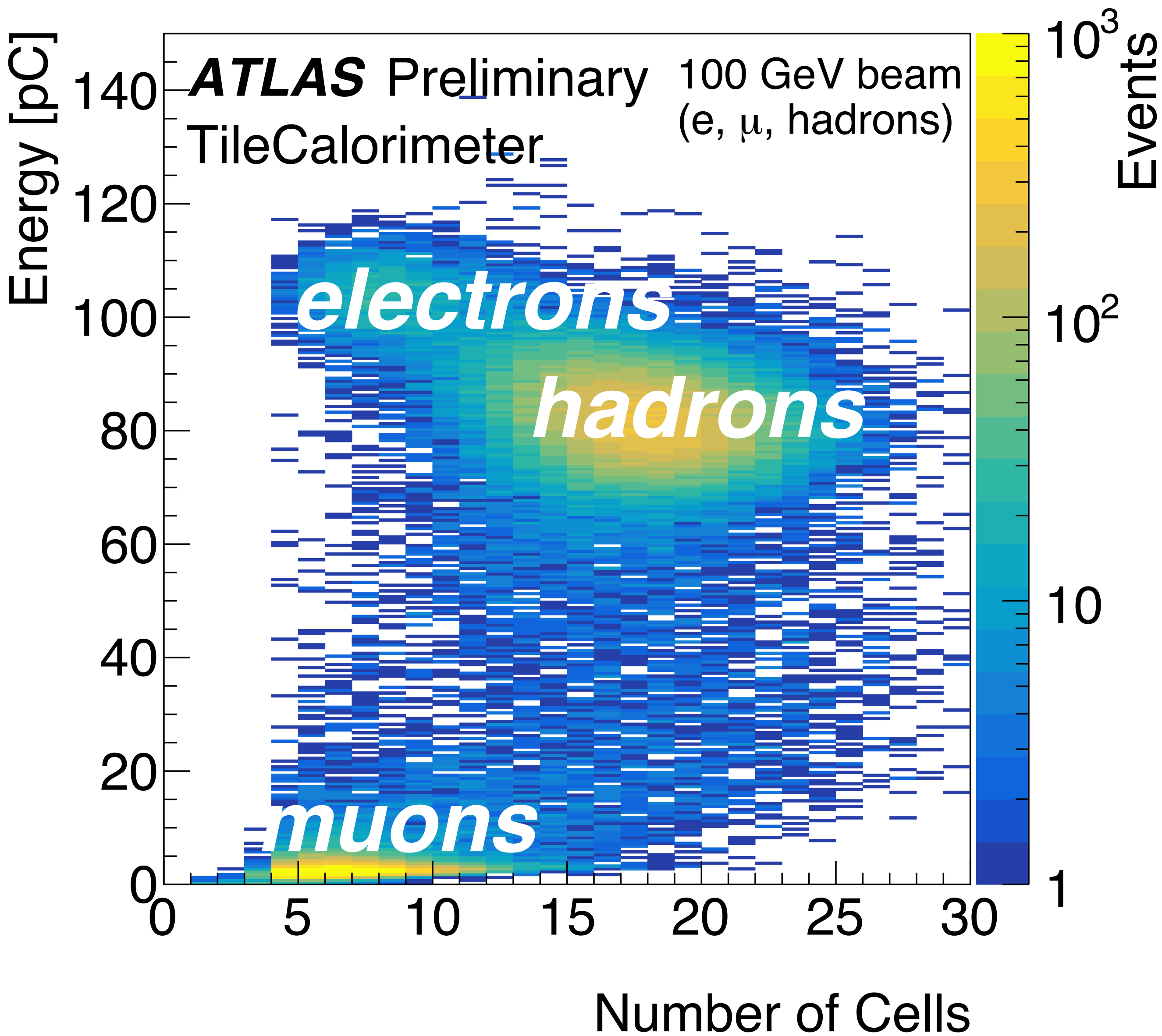
Test beam control room

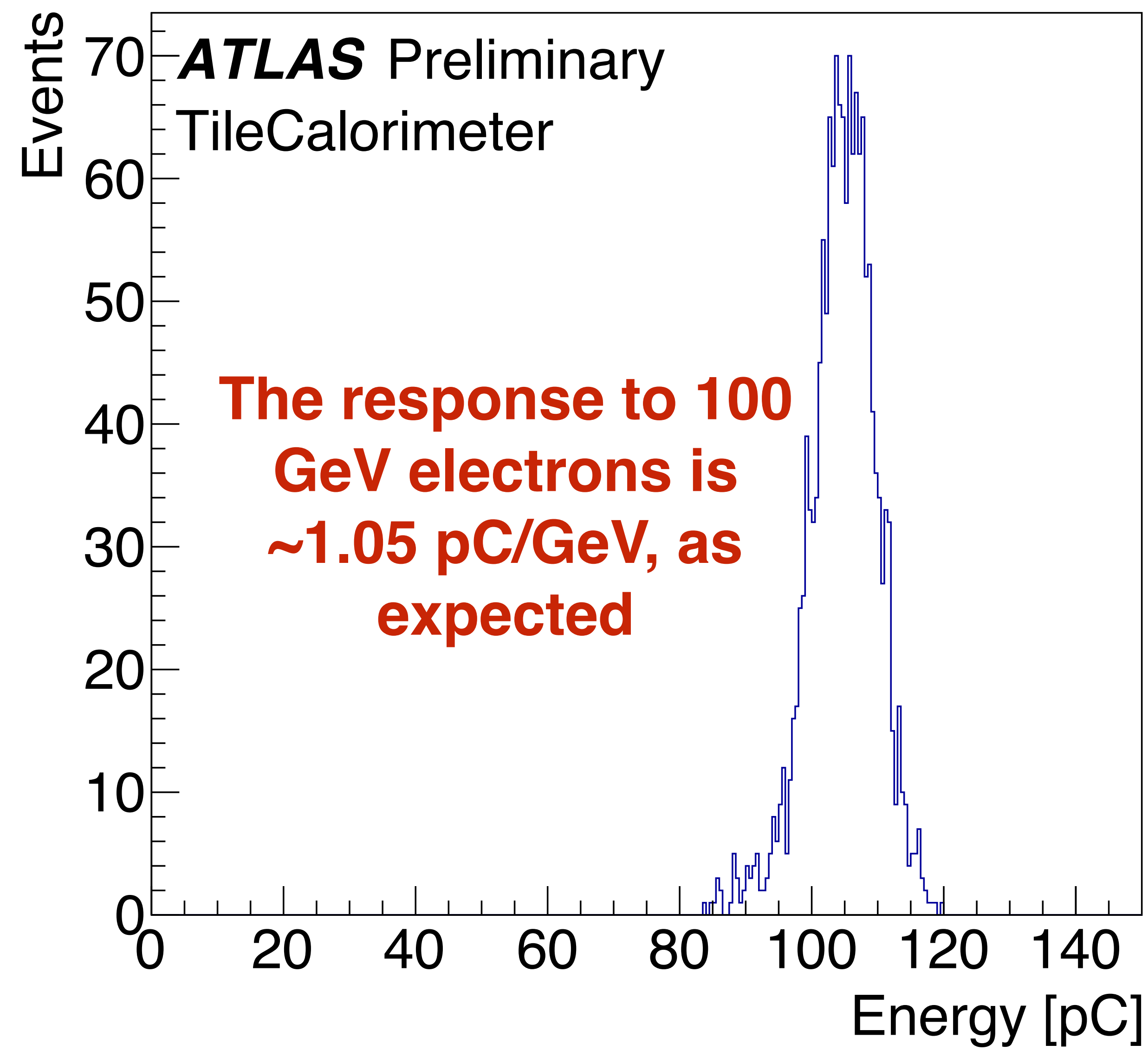


Results (3-in-1): 100 GeV mix of μ, e, and hadrons

Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileTestBeamResults

Data collected with the 3-in-1 demo during the test beam in Oct-Nov 2016 test beam



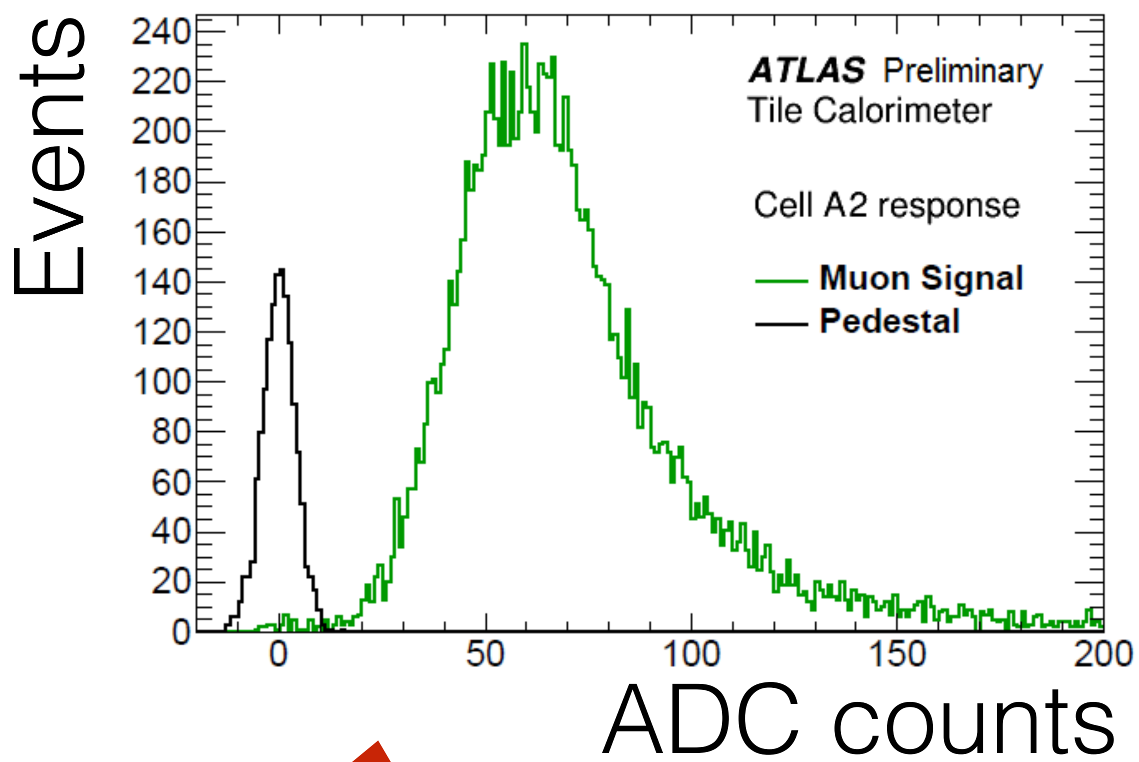


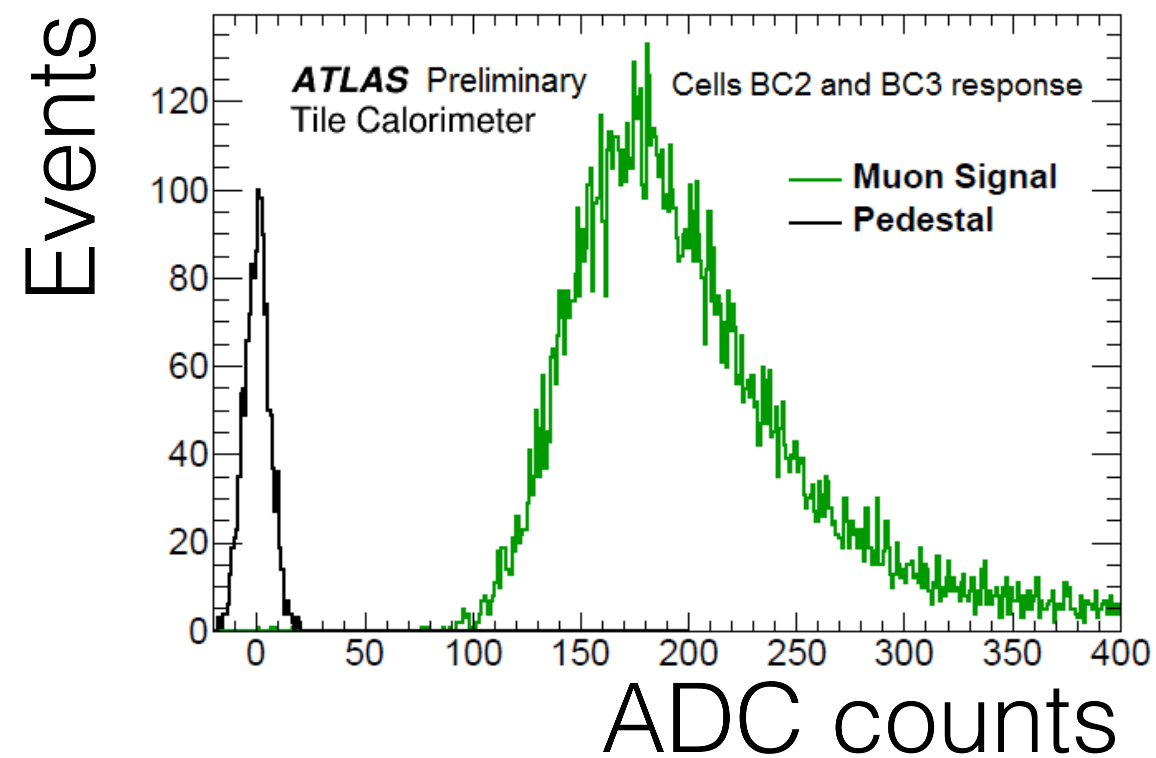
The response to 100 GeV electrons is ~1.05 pC/GeV, as expected

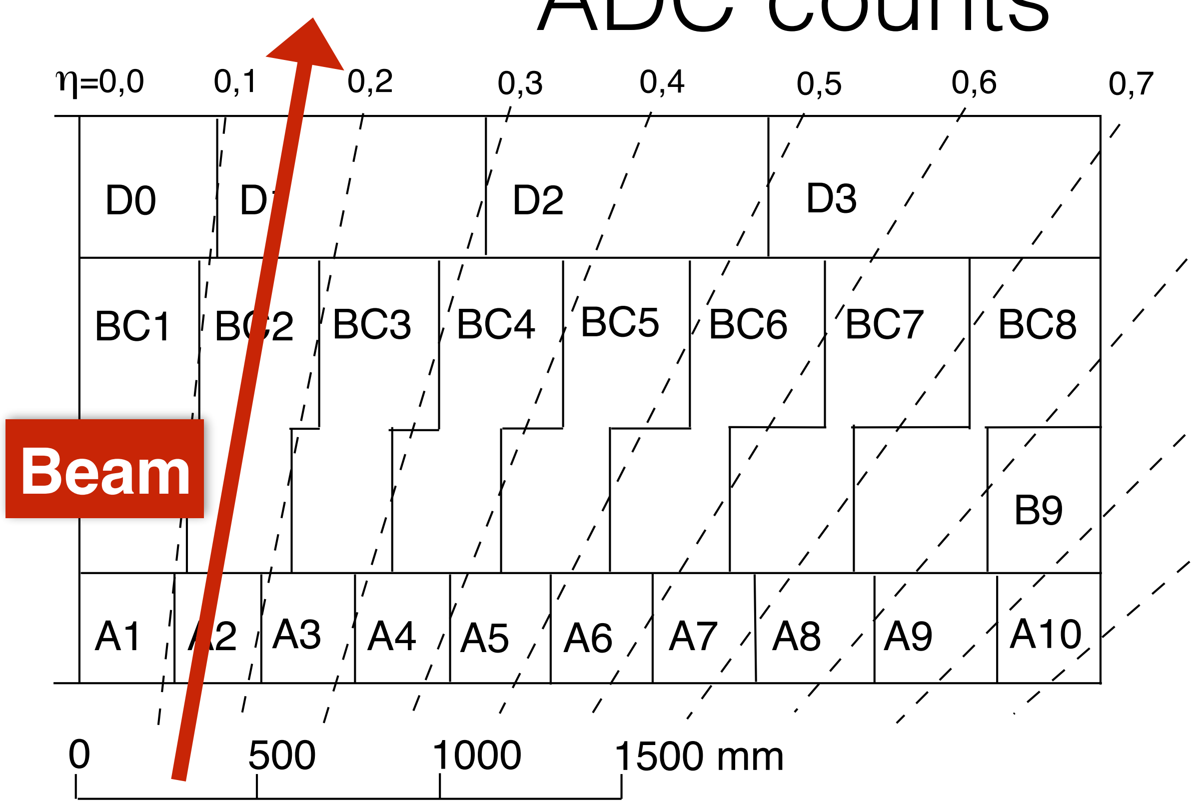
Results: 100 GeV muons

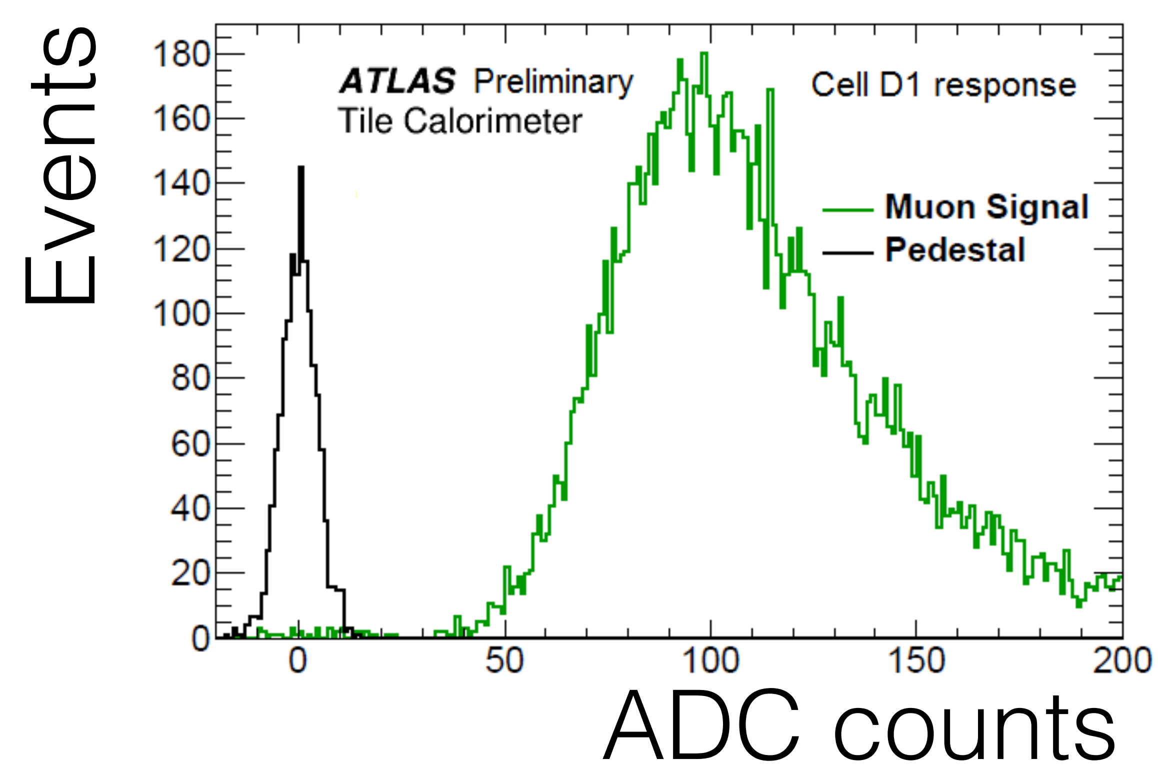
Source: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileTestBeamResults

Data collected with the 3-in-1 demo during the test beam in Oct-Nov 2016 test beam









Conclusions

- TileCal is performing well at 13 TeV
  - Results of the calorimeter response to single hadrons (E/p) at 13 TeV were presented
- All TileCal readout electronics to be replaced for the high luminosity LHC upgrade
  - Necessary for TileCal to be compatible with the new digital ATLAS readout and trigger architecture
- Status of the upgrade
  - A decision was recently made to proceed with the “upgraded 3-in-1” front-end electronics option
  - Tile backend electronics under design and prototyped
- Goals of the test beam program
  - Evaluate the performance of the upgrade electronics
  - Measurements of electrons, muons, and low energy hadrons

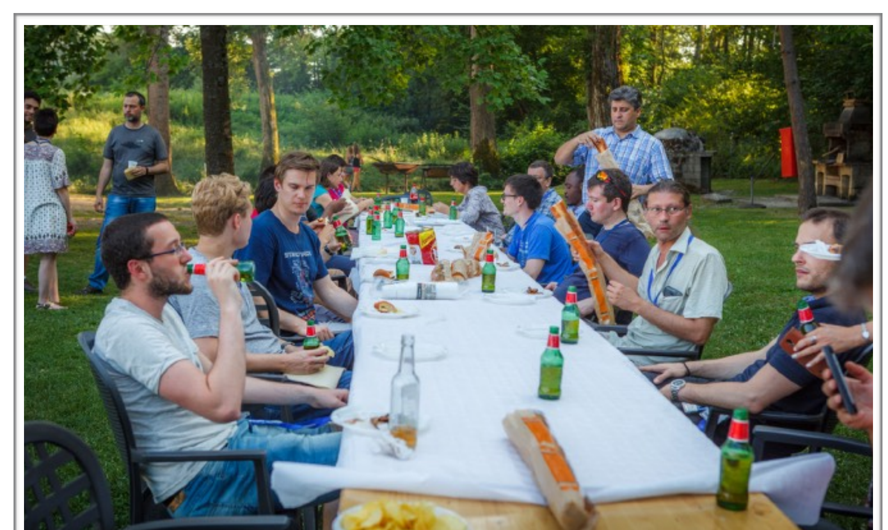
Huge thanks to the ATLAS TileCal team :)







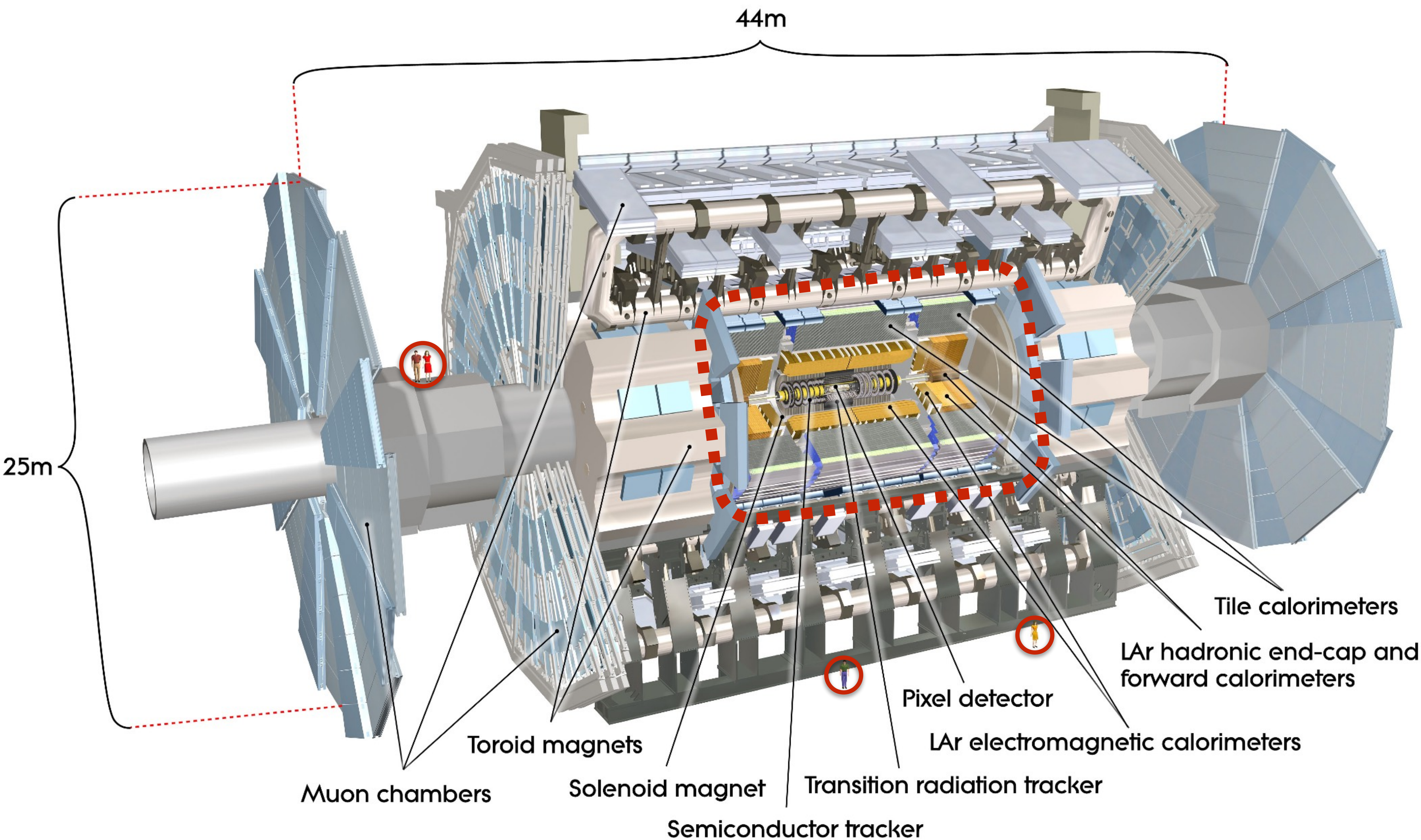


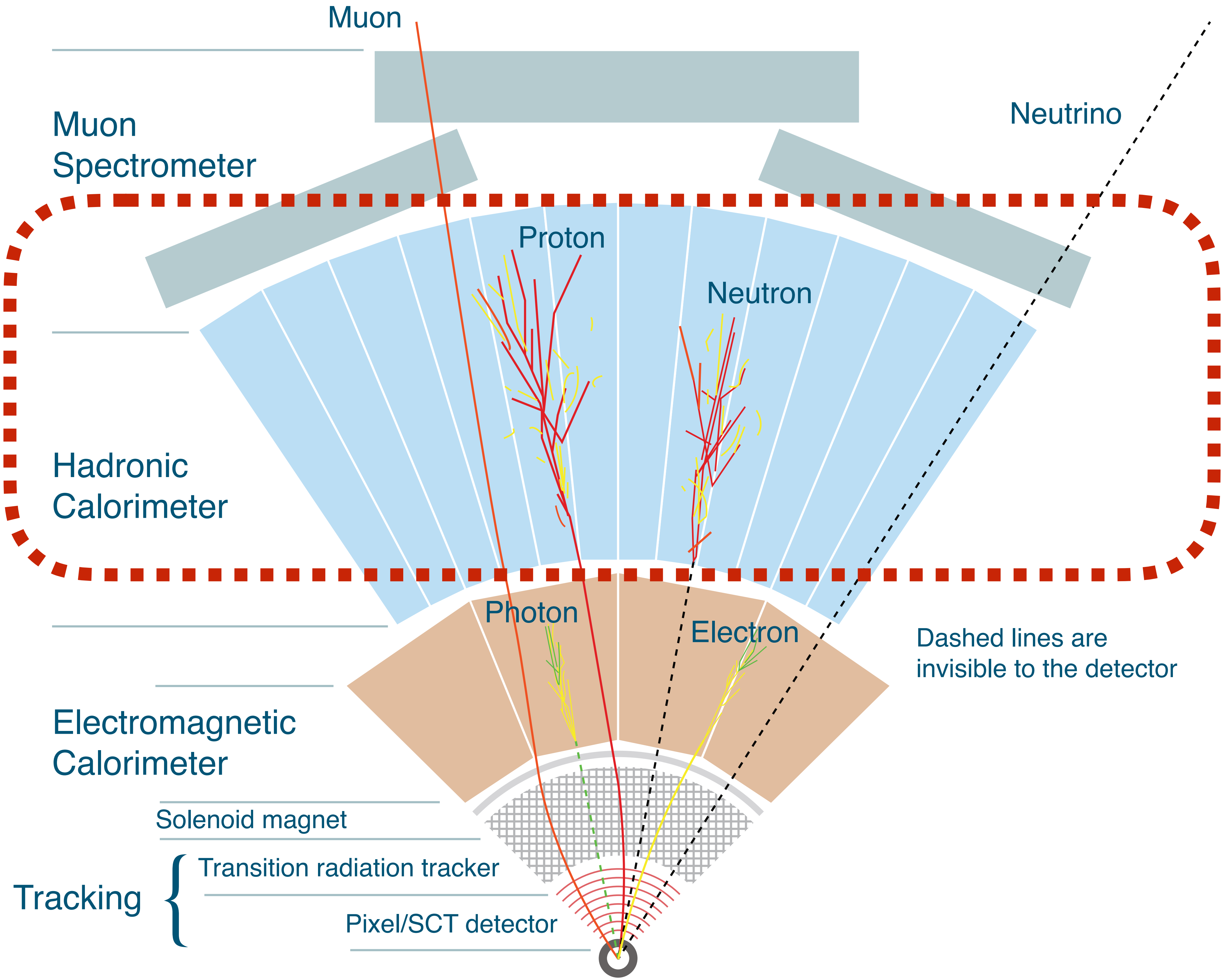

Thanks for your attention!

Backup material

The ATLAS Experiment

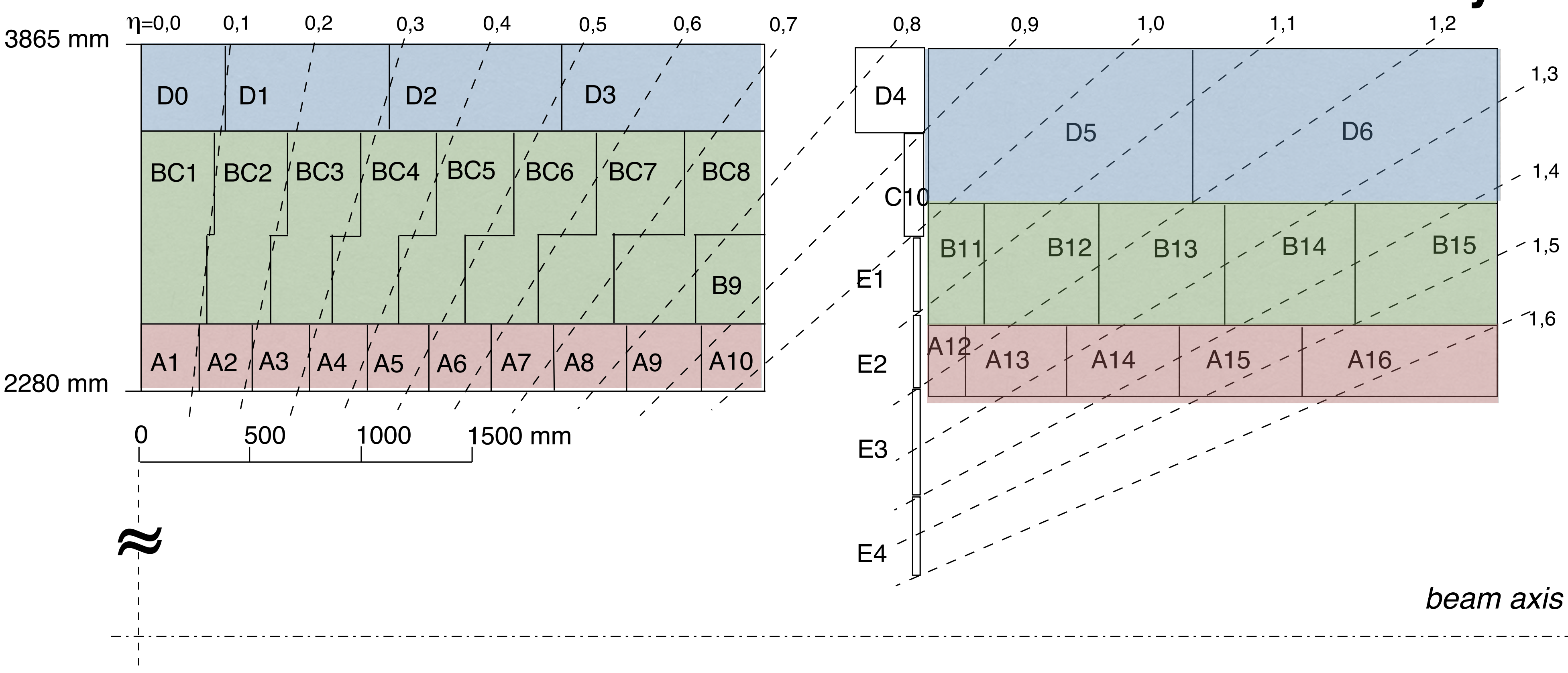


The ATLAS Experiment



TileCal readout

3 layers in transverse direction

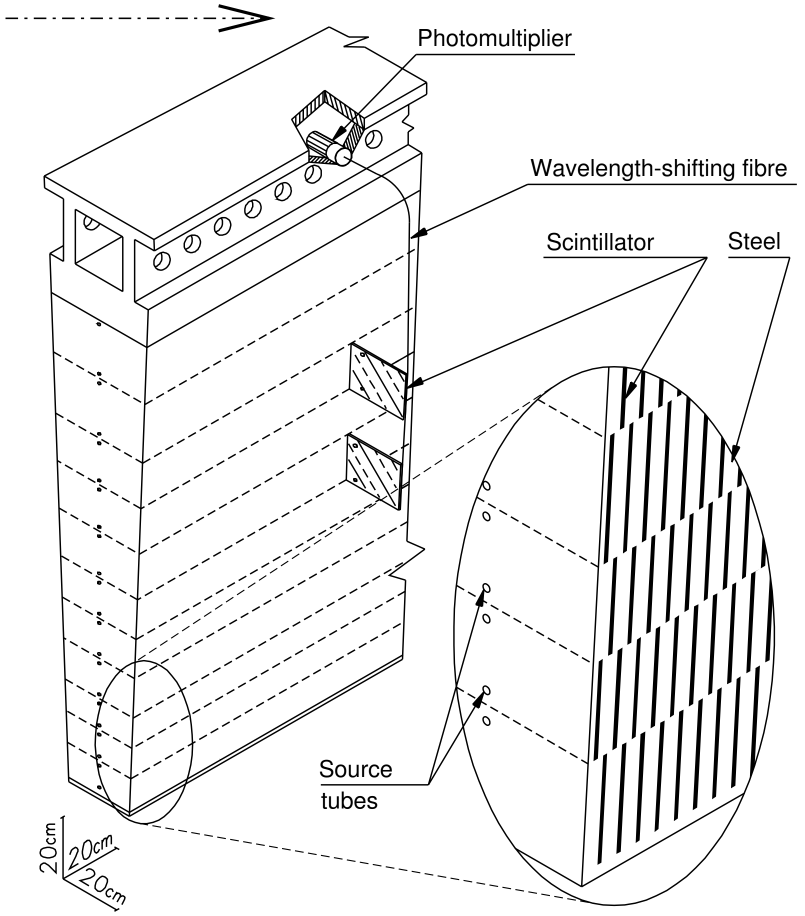


"D"-cells

"BC"-cells

"A"-cells

	Channels	Cells	Trigger Outputs
Long barrel	5760	2880	1152
Extended barrel	3564	1790	768
Gap and crack	480	480	128
MBTS	32	32	32
Total	**9836**	**5182**	**2080**

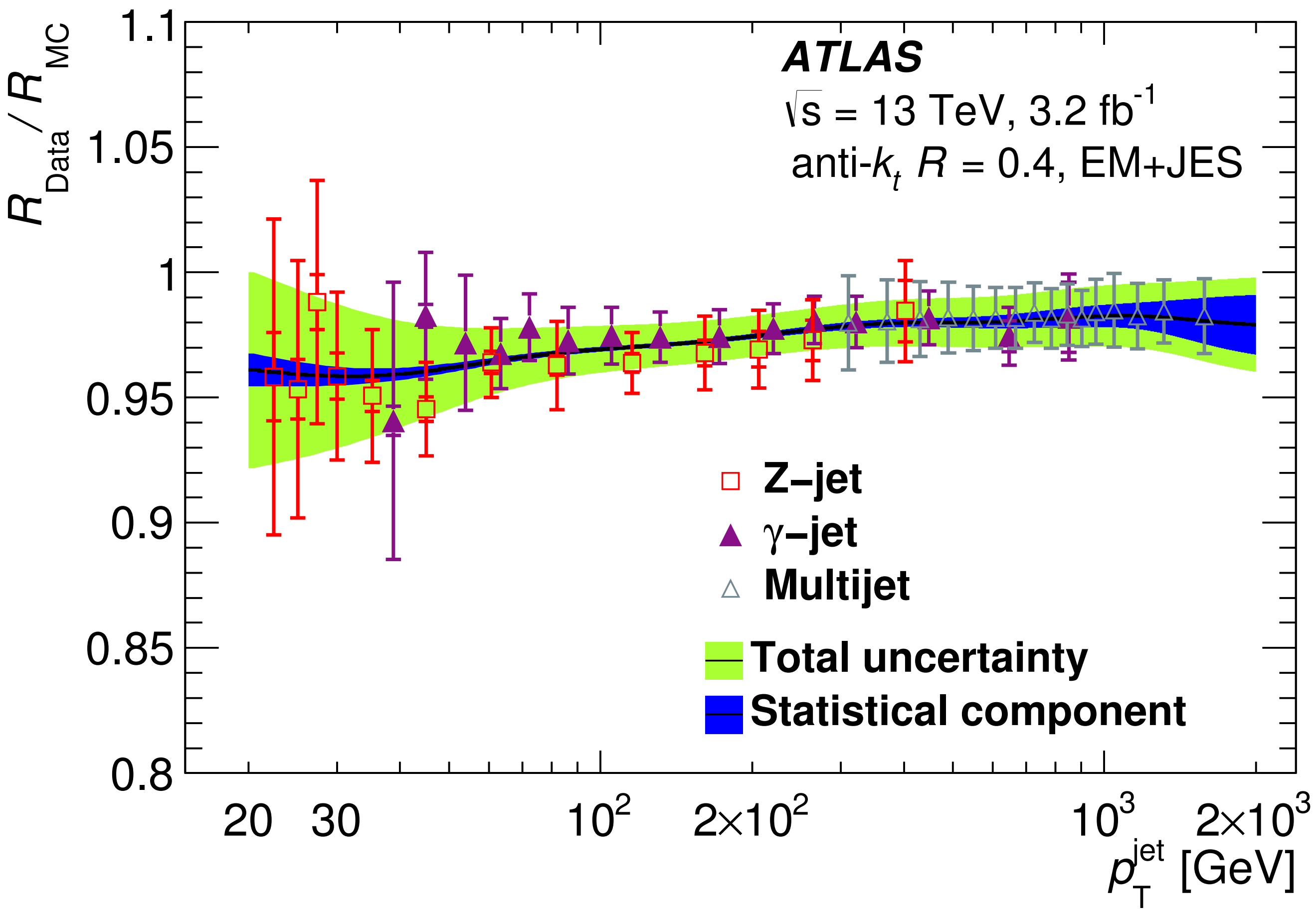


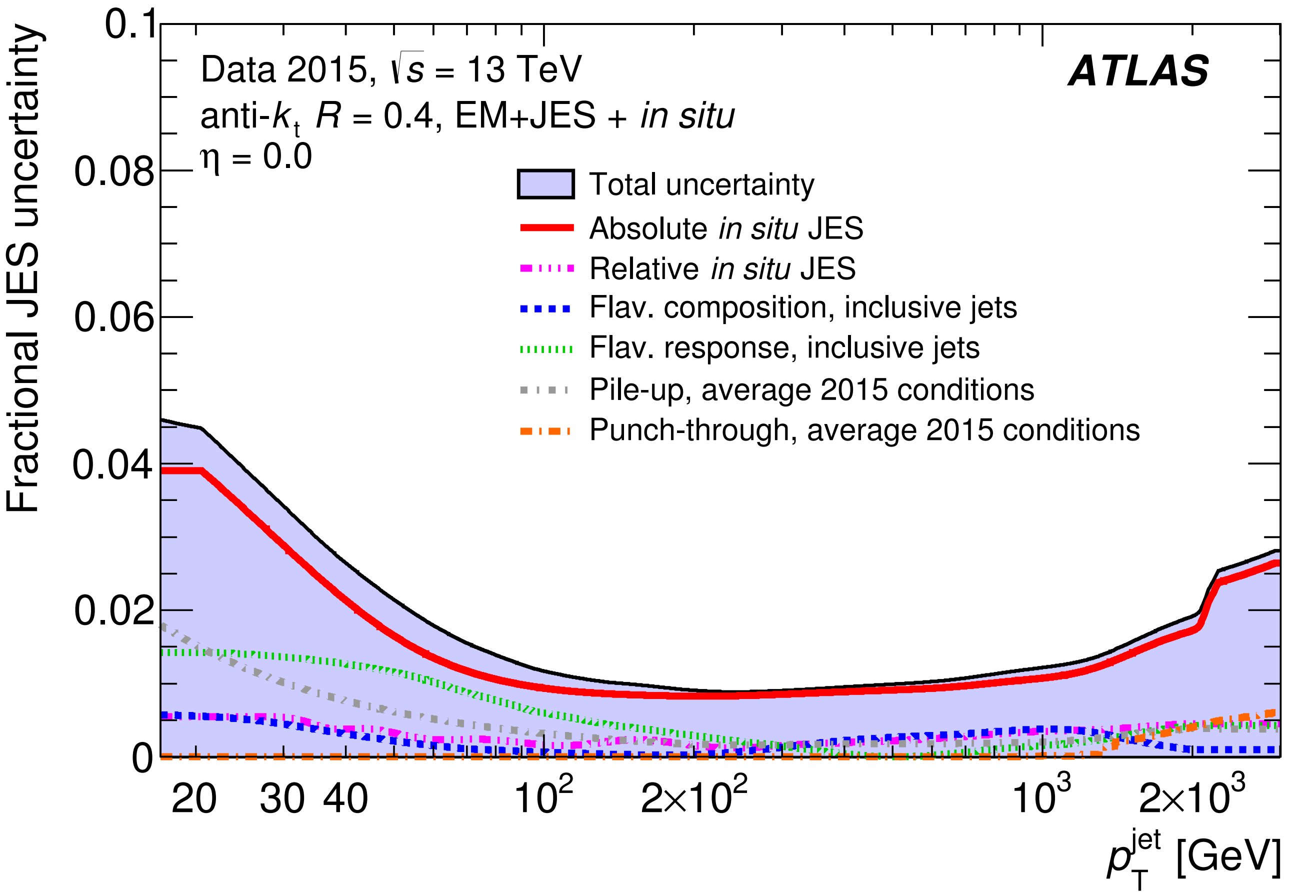
E/p — Event and track selections

- Track isolation requirement
  - No other tracks are allowed within a cone of $\Delta R < 0.4$ of the selected track
- Track-cluster/cell matching
  - Energy deposits associated with a cluster are matched to a track if $\Delta R < 0.2$ between the cluster/cell and the track (extrapolated to the most energetic sampling layer of a cluster)
- Reject background from neutral hadrons and muons and ensure that a significant fraction of the total energy is deposited in TileCal
  - **Track $p > 2$ GeV and $|\eta| < 1.7$ GeV**
    - Increase fraction of particles depositing significant energy fraction in TileCal)
  - **$E_{EM} < 1$ GeV**
    - Energy deposited in EM calo compatible with minimum ionizing particle
  - **$E_{Tile} / E_{Tot.} > 0.7$**
    - Reject background contamination from muons

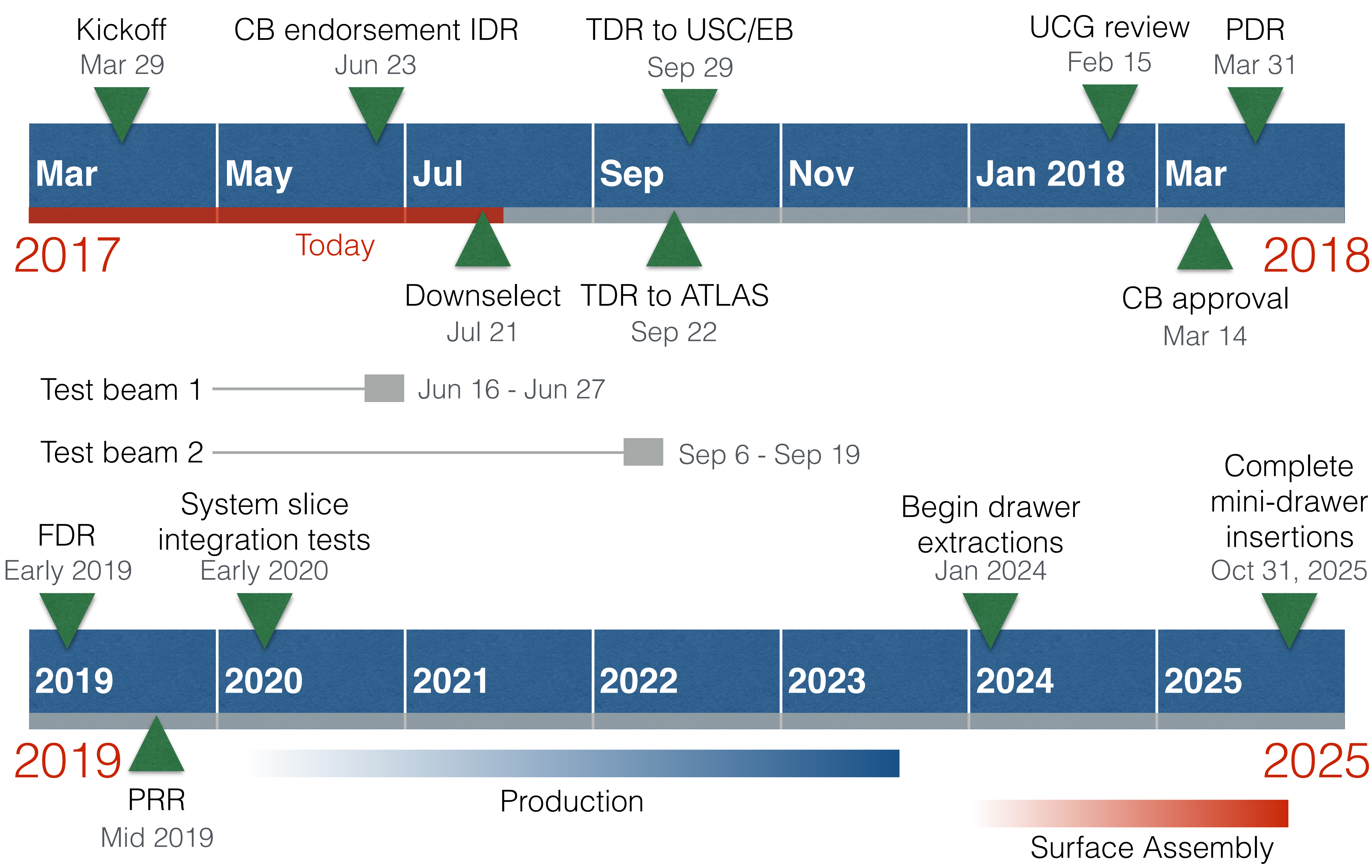
ATLAS Jet Energy Scale (JES) @ 13 TeV

arXiv:1703.09665

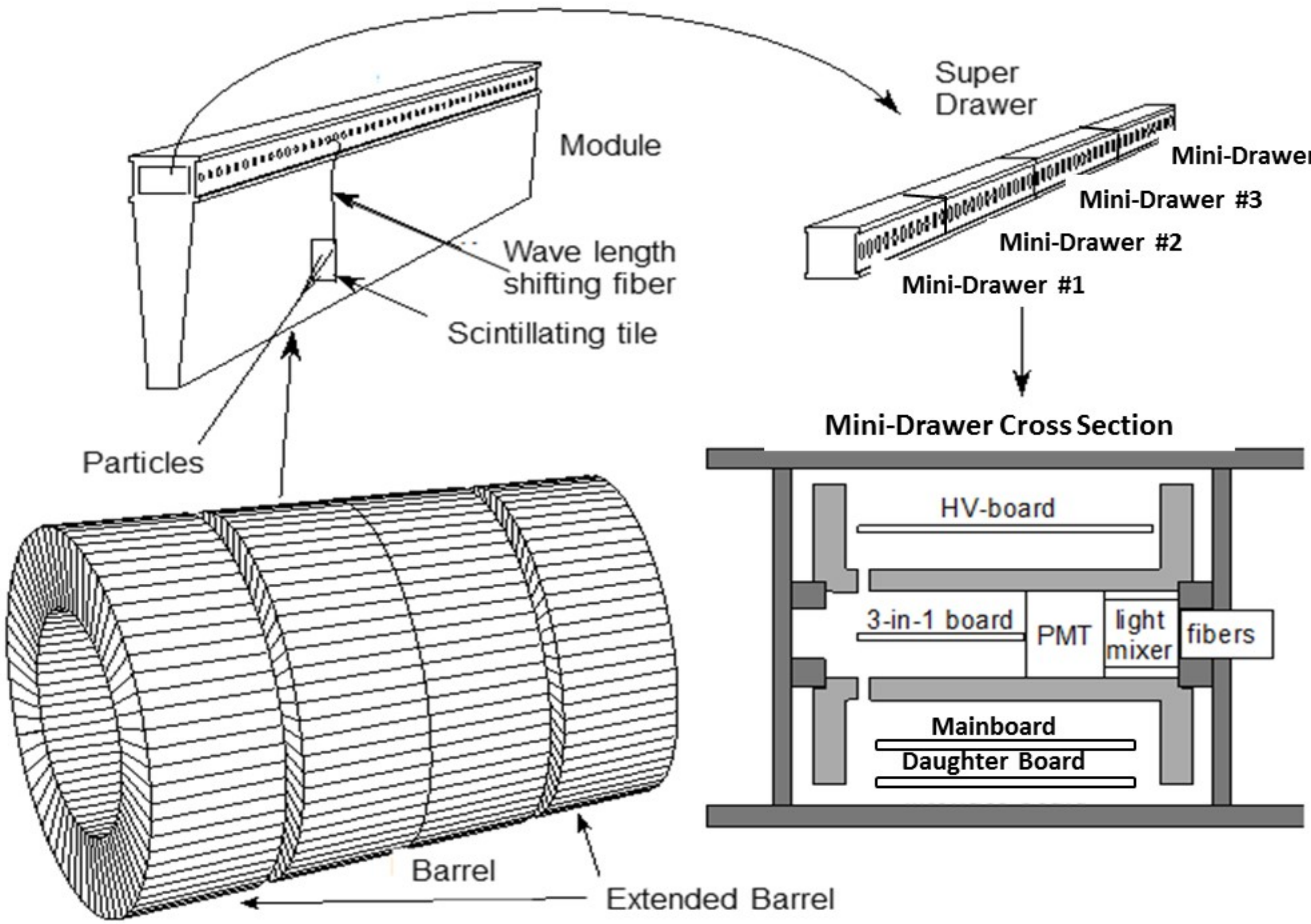




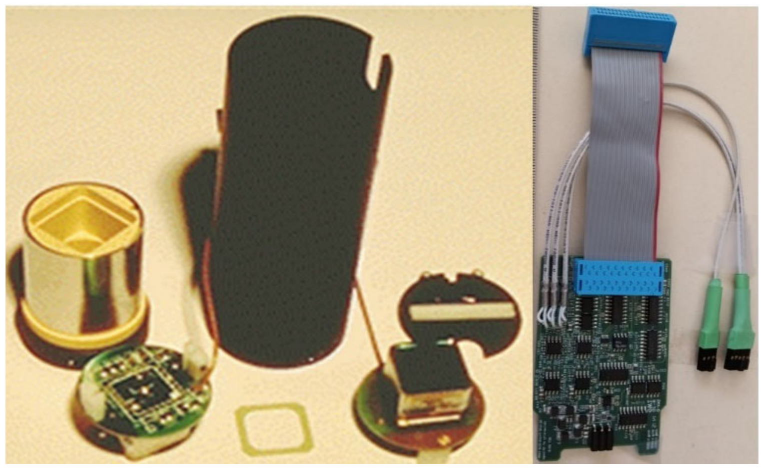
Tile upgrade milestones



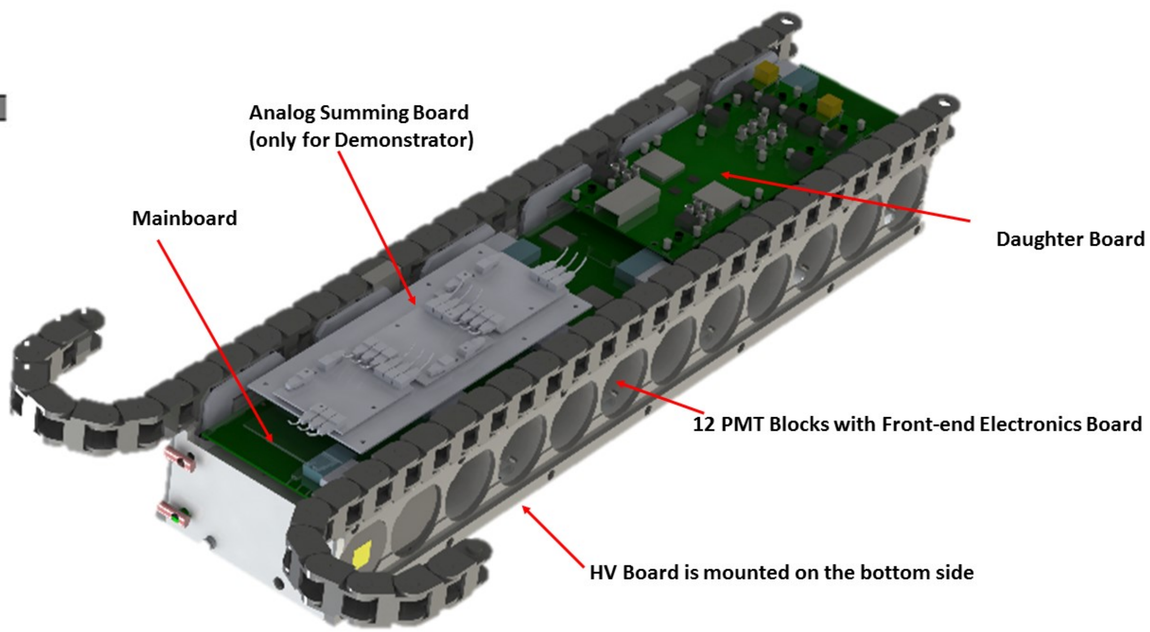
On-detector electronics



On-detector electronics drawers



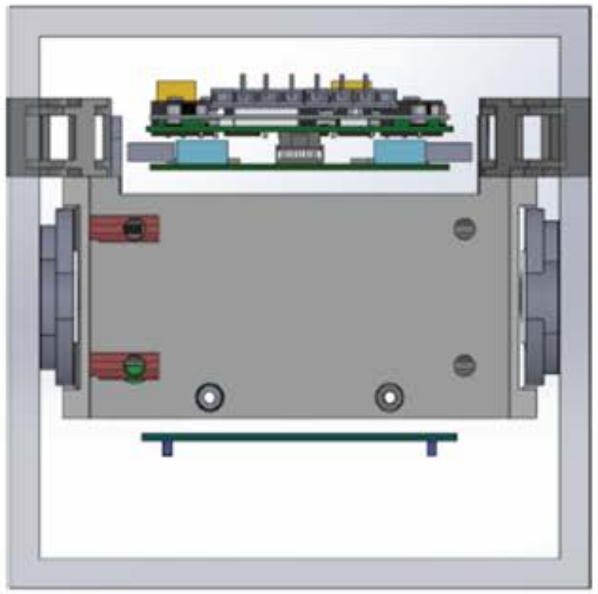
PMT with 3-in-1 card



Tile Cal mini-drawer

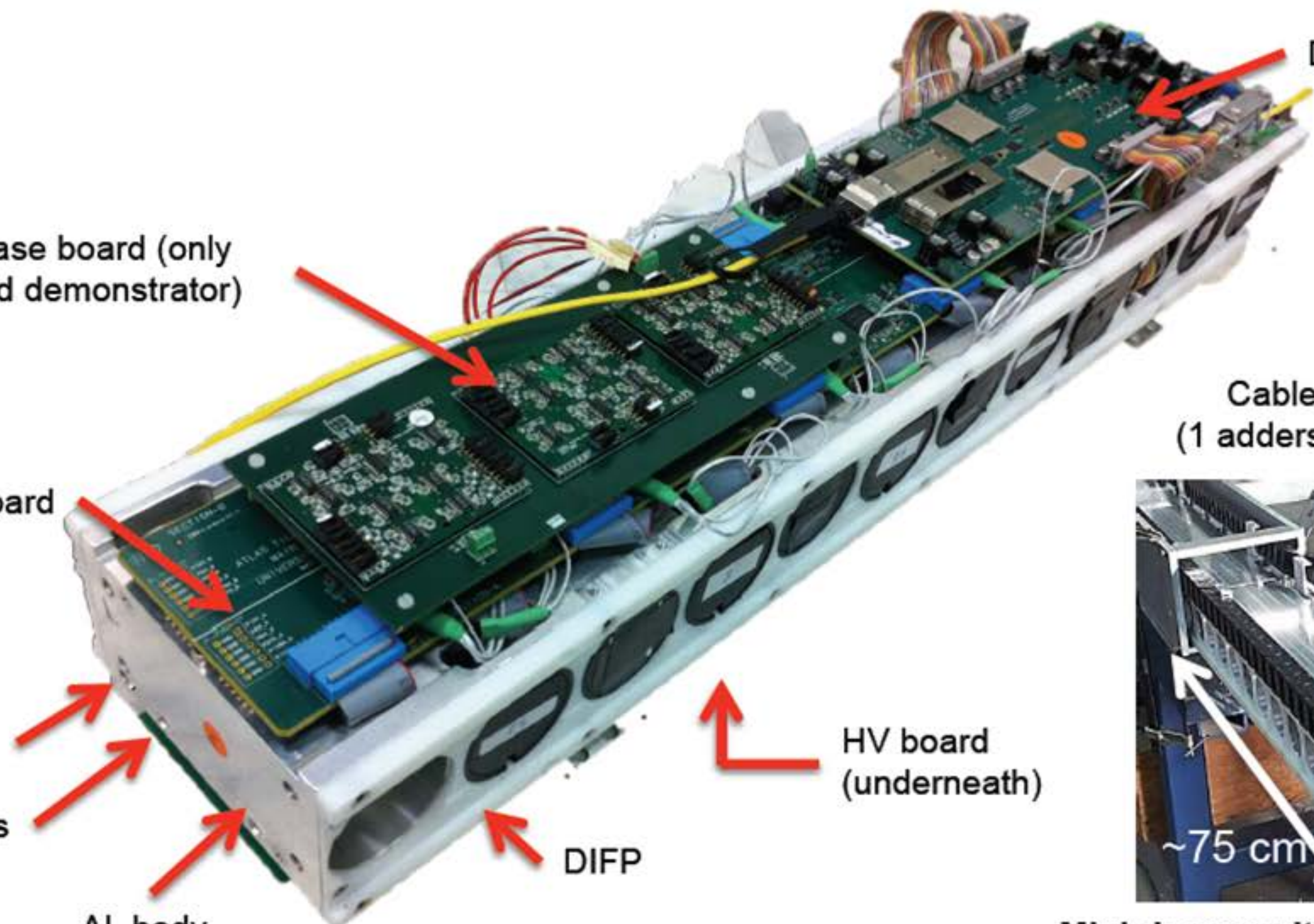
Demonstrator mini-drawer

- Super-drawer demonstrator is composed of 4 mini-drawers, each one containing
  - 12 front-end boards: 1 out of 3 different options
  - 1 main-board: for the corresponding FEB option
  - 1 daughter board: single design
  - 1 HV regulation board: 1 out of 2 different options
  - 1 adder base board + 3 adder cards: for hybrid demonstrator

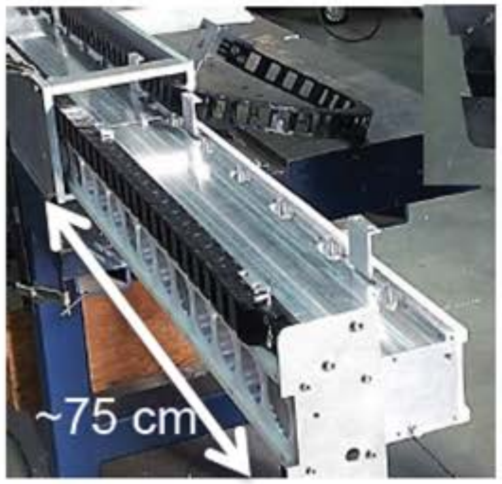


Cross section of a mini-drawer

Required assembly of 45 PMT blocks with new active dividers

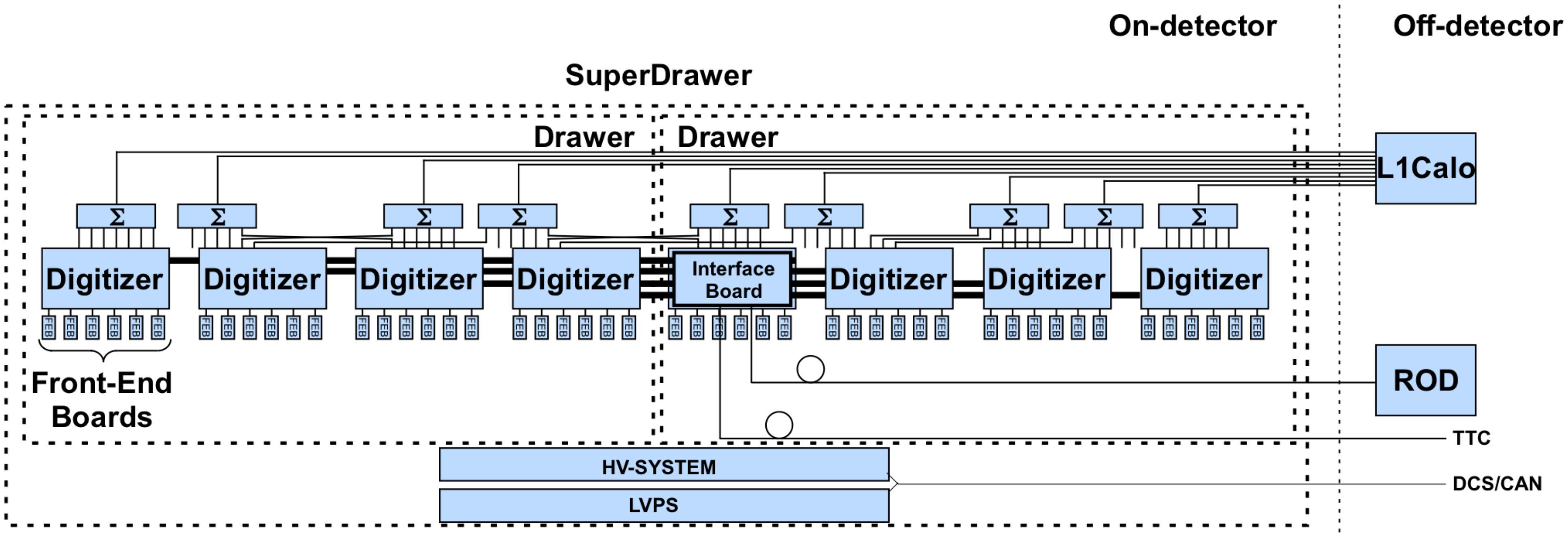


Cable carrier (1 adders, 1 digital)

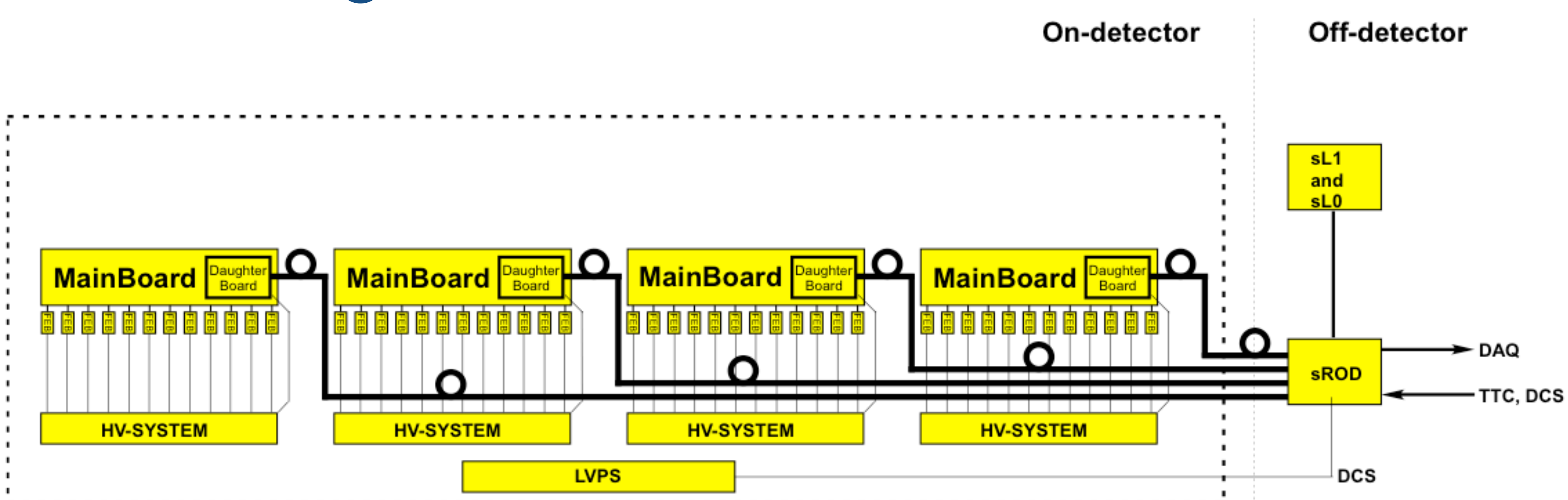


Mini-drawer with cable carriers

Current drawers vs. new mini-drawers



Current organization of electronics in two drawers



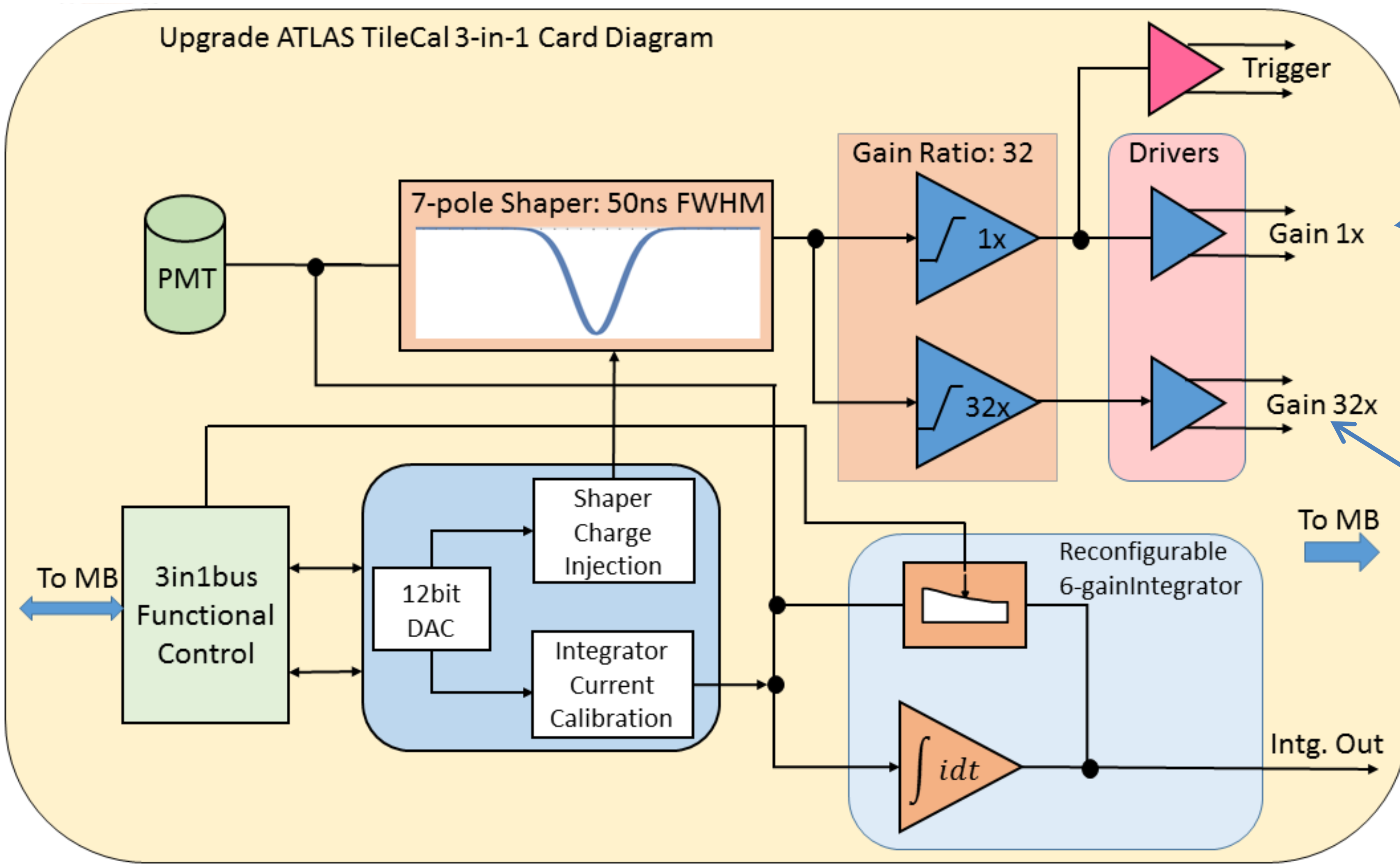
Upgrade: organization of electronics in four mini-drawers

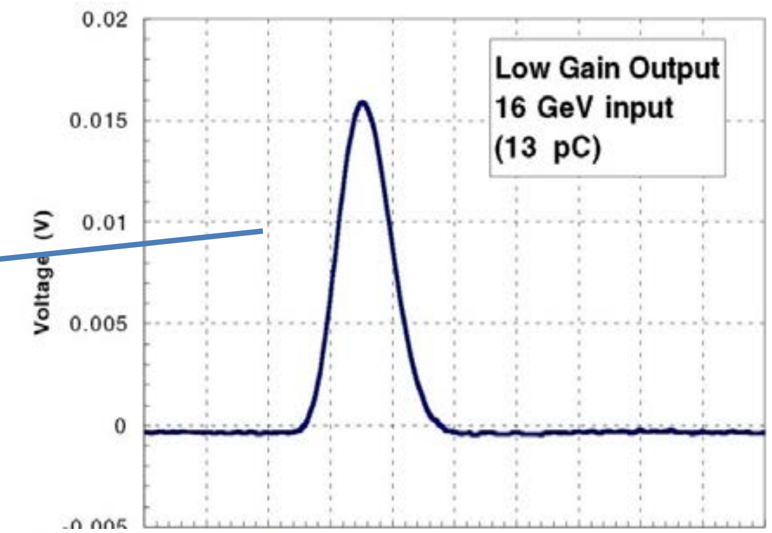
Front-end electronics options

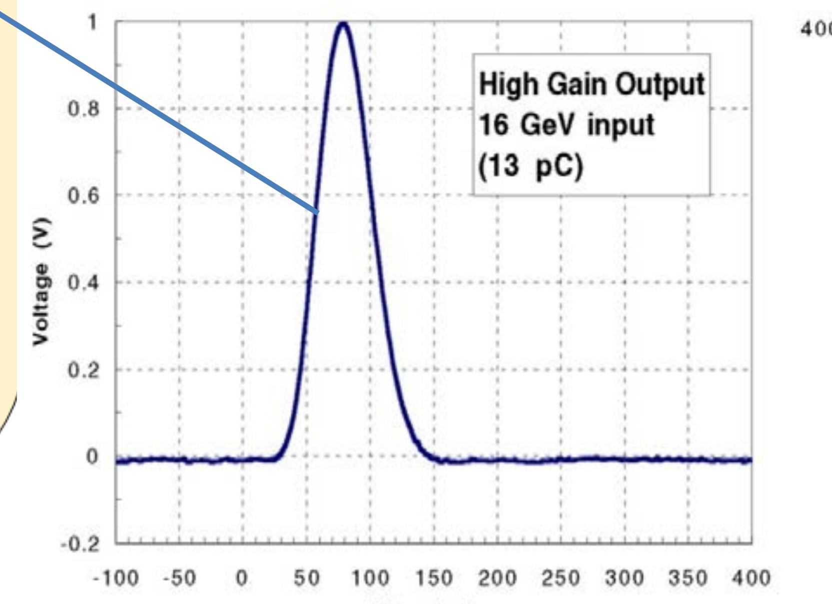
- Upgraded 3-in-1
  - Shaped pulse (50 ns FWHM)
  - 17 bit dynamic range in two gain ranges (12 bit ADC)
  - Discrete components, lower electronics noise than present system
  - **Advantages:** proven technology, compatible with legacy system and current analog TileCal trigger (demonstrator can be installed before HL-LHC)
- QIE (**C**harge **I**ntegrator and **E**ncoder)
  - 25 ns gated integrator with amplitude threshold time measurement
  - ASIC, dynamic range achieved through 4 non-linear gain ranges
  - **Advantages:** proven radiation hard technology, has been used in many other experiments (including CMS and CDF)
- FATALIC (**F**ront-end **AT**l**A**s ti**L**e **I**ntegrated **C**ircuit)
  - Shaped pulse (45 ns FWHM)
  - ASIC, dynamic range achieved in three gain ranges
  - **Advantages:** fewer components, potential for higher radiation tolerance

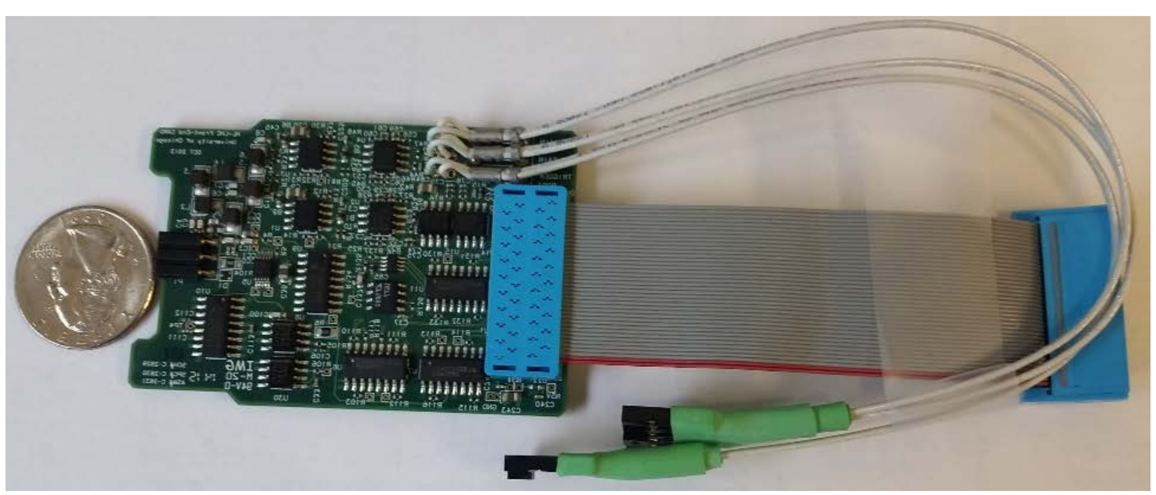
A decision was recently made to proceed with the upgraded 3-in-1

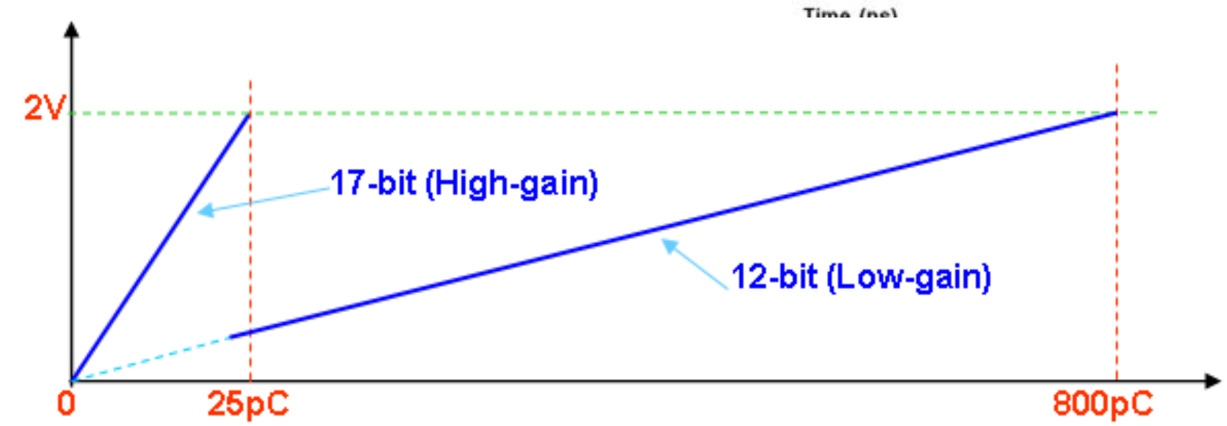
Schematic of 3-in-1 front-end board





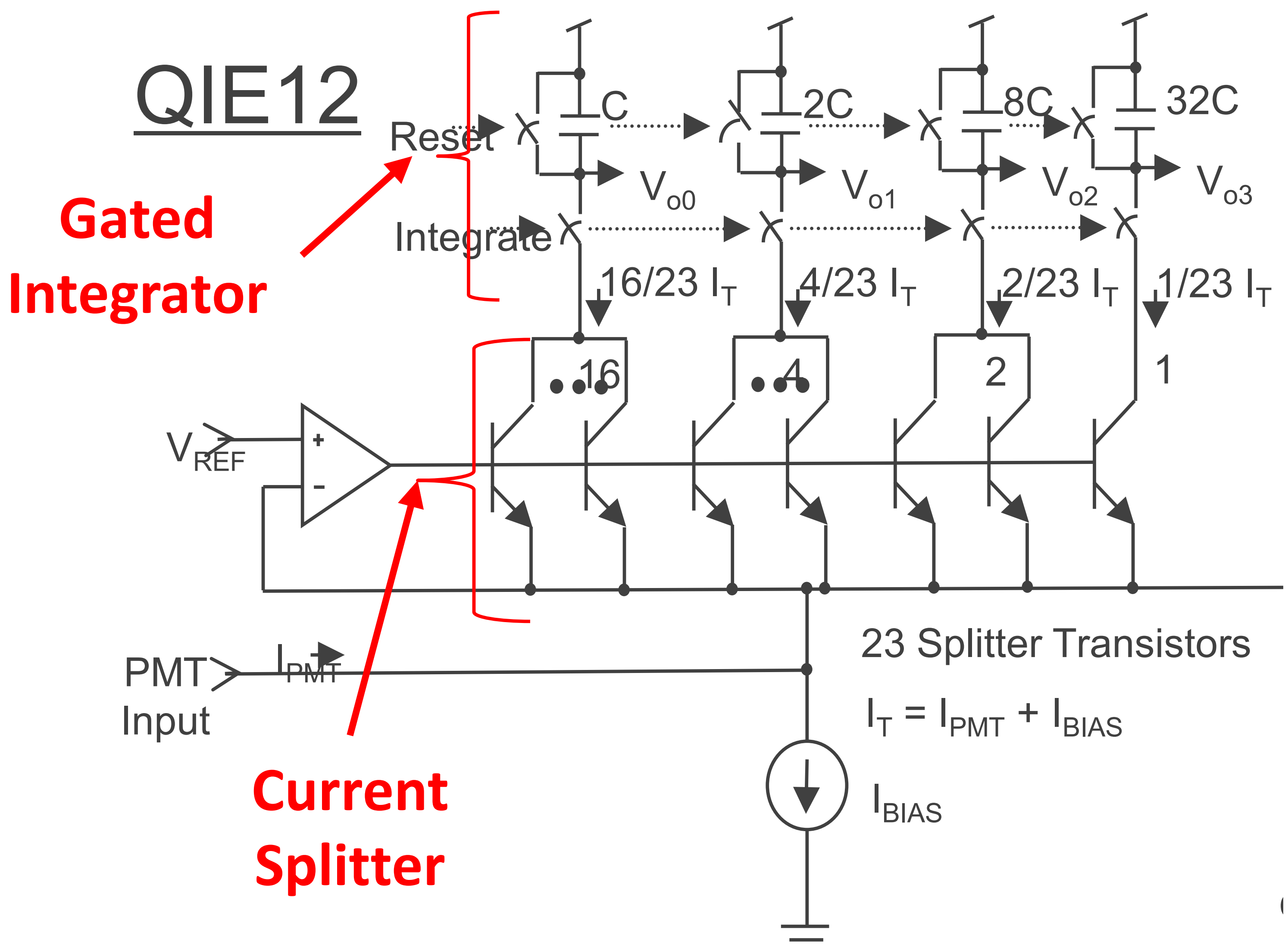






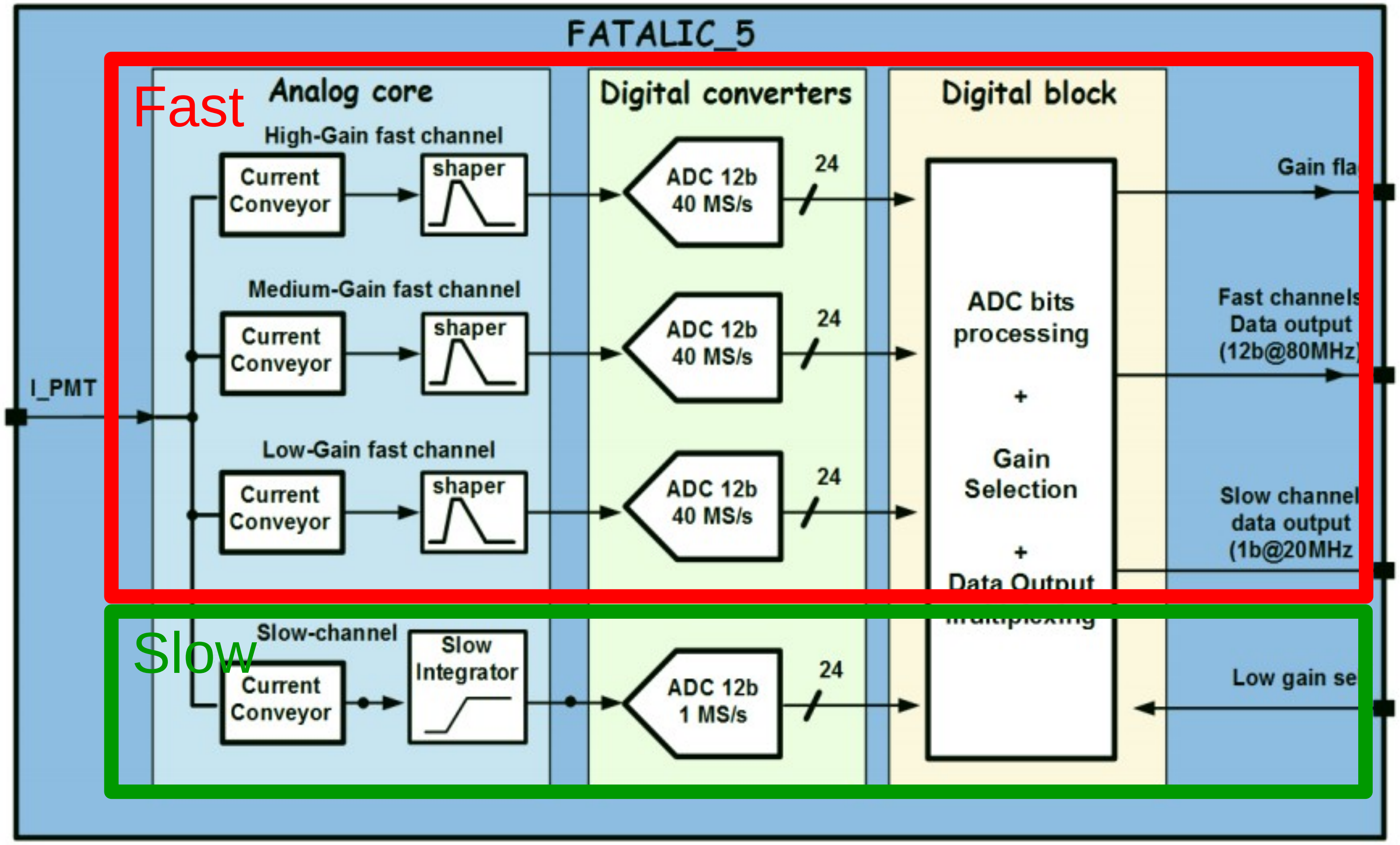
Schematic of the QIE front-end board

- The PMT current is integrated in a bank of capacitors
- The capacitors are time-multiplexed for deadtimeless operation at 40 MHz
- The current splitter is used to achieve the required dynamic range of > 17 bits
- The QIE12 ASIC is designed to be radiation tolerant and tailored for TileCal



Schematic of the FATALIC front-end board

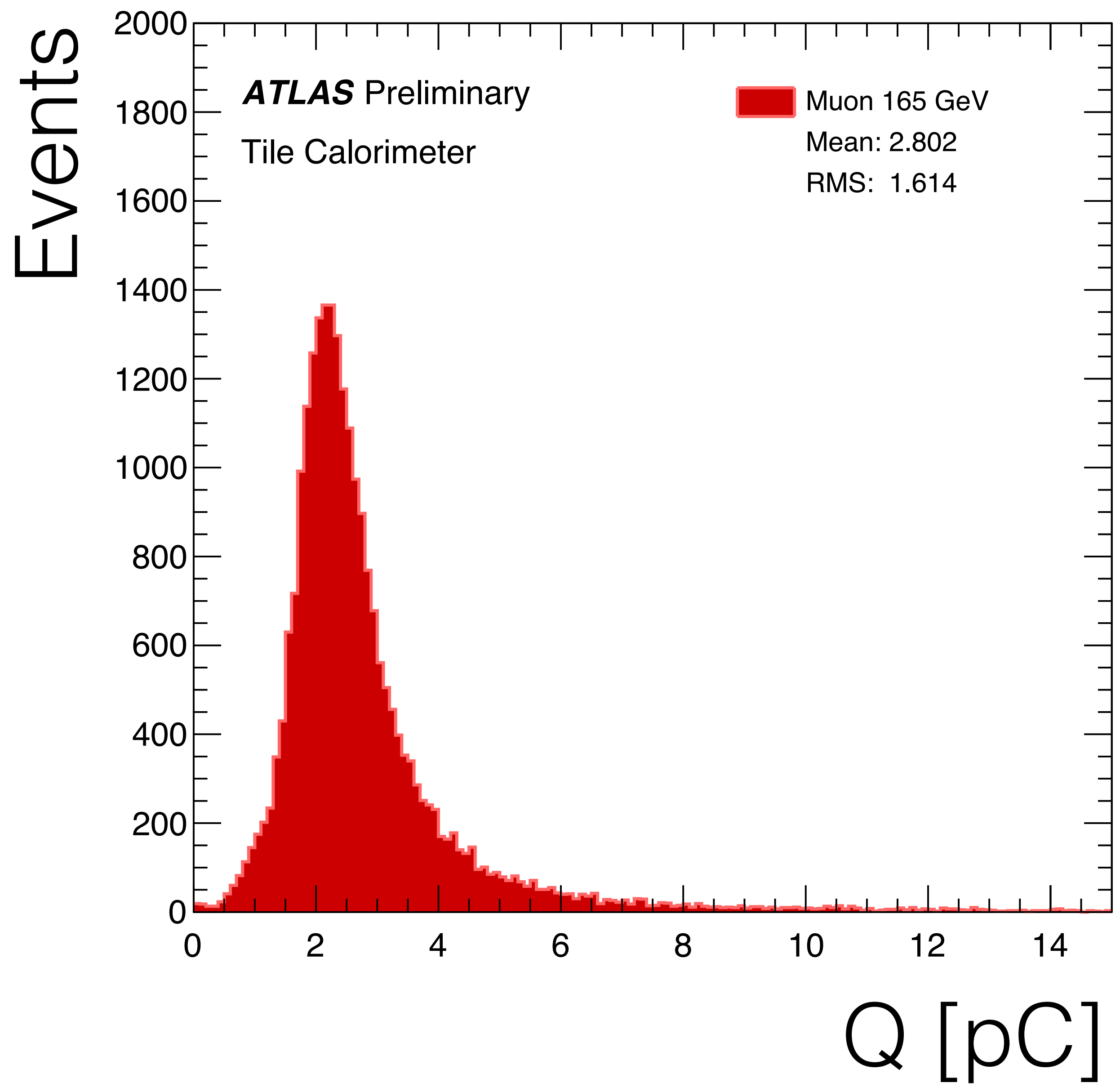
- ASIC that includes all the reconstruction elements
- Optimal energy resolution with 3 gains (x64, x8, x1) + dynamic gain switch
- Currently a Main Board with 4 FPGAs, 3 channels/FPGA + Daughter Board

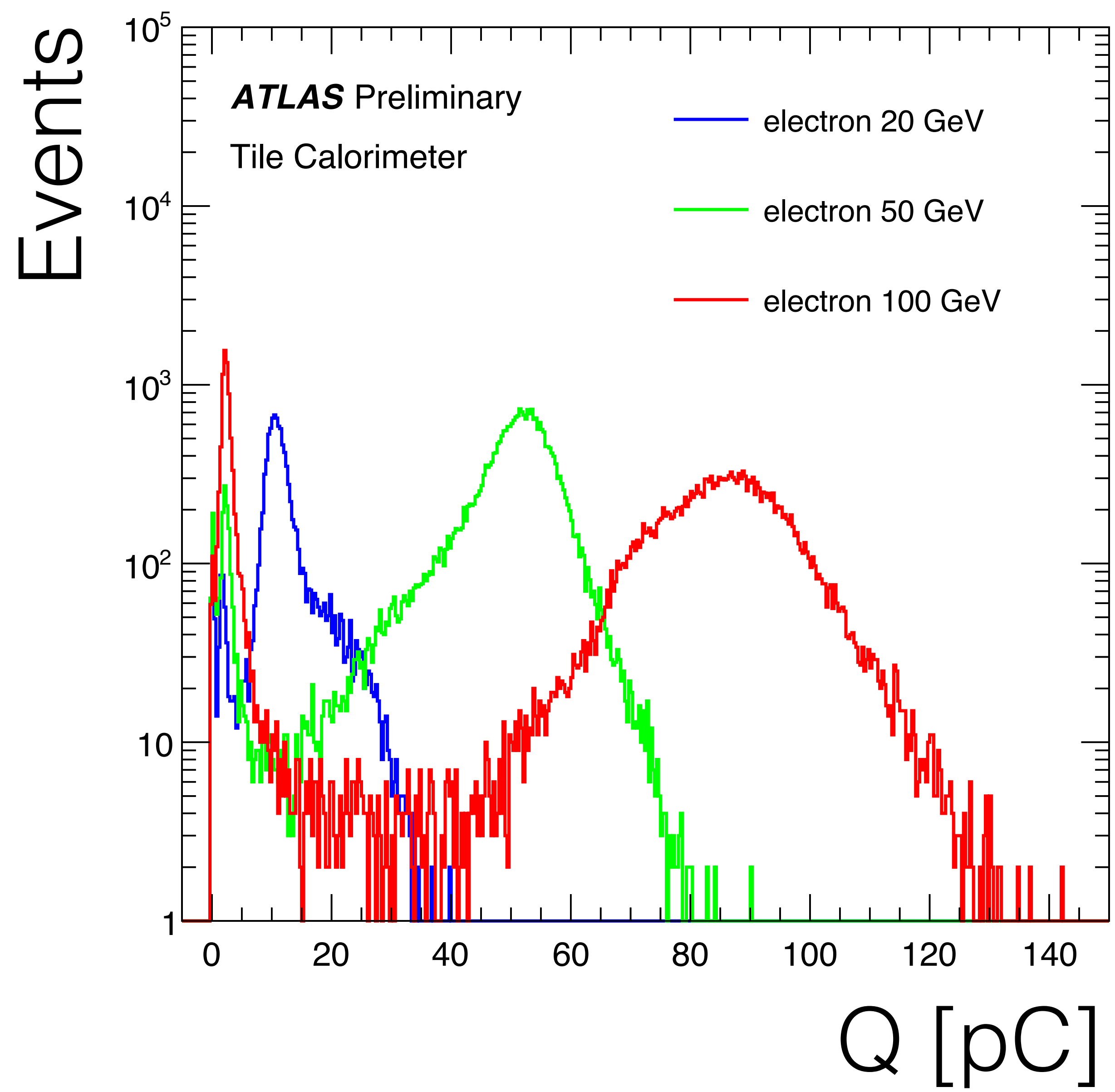


Test beam results: 165 GeV muons

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileTestBeamResults

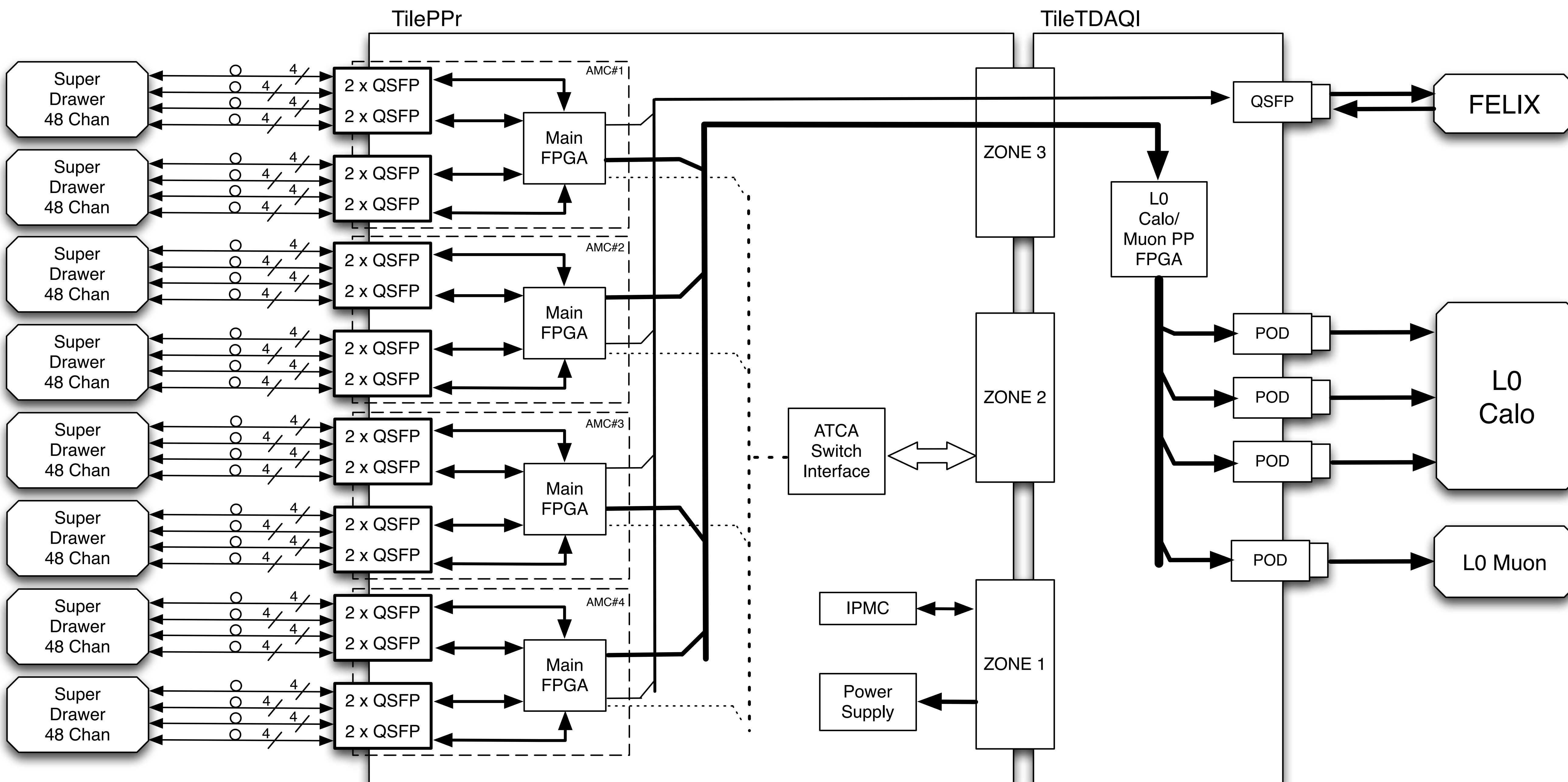
Data collected with the FATALIC demo during the test beam in June 2017





TilePPr: schematic

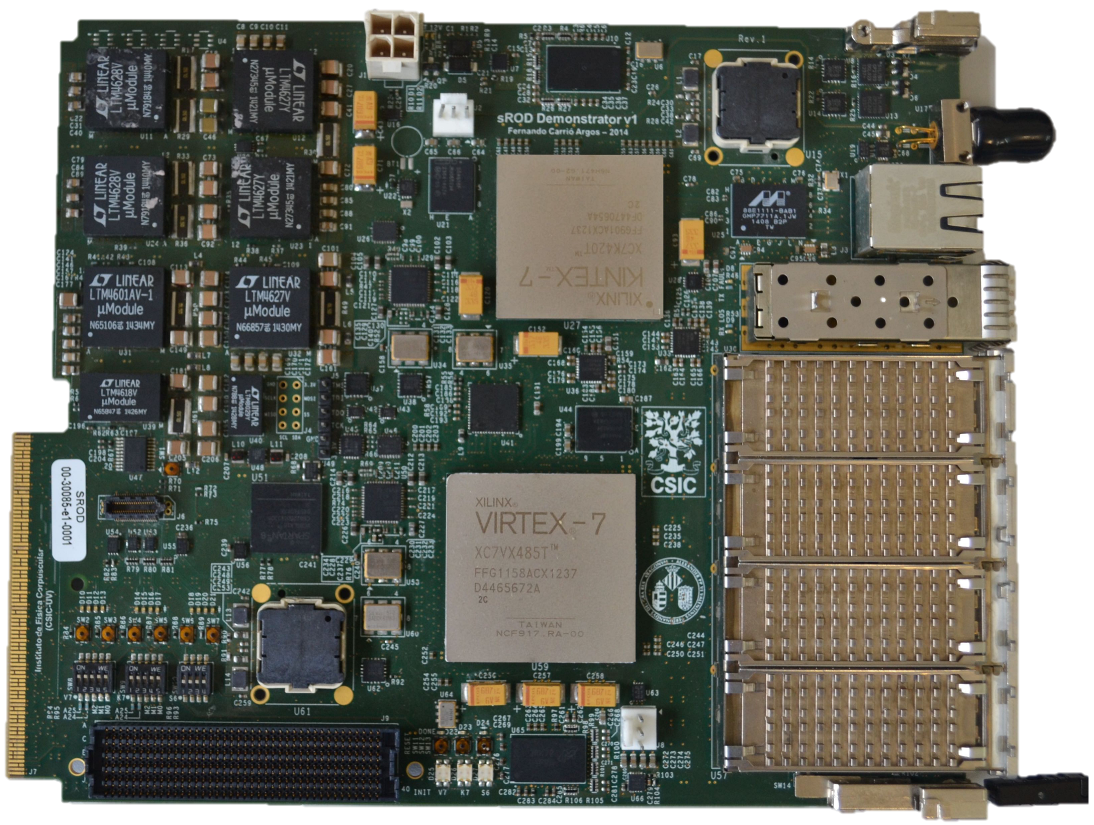
Source: ATLAS-TILECAL-PROC-2015-025



TilePPr: production

Source: ATLAS-TILECAL-PROC-2015-025

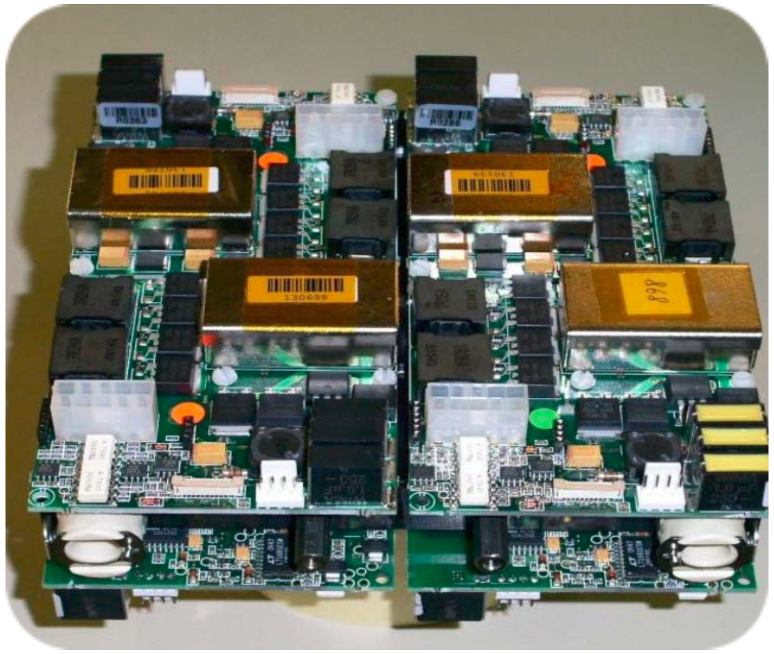
- 6 working TilePPr prototypes
  - 4 TilePPrs at Valencia laboratories
  - 2 TilePPrs at the TestBeam area: One for 3-in-1 demonstrator and a shared one for QIE and FATALIC
- 2 newly assembled TilePPrs are undergoing testing
- Plan to assemble 2 more TilePPrs

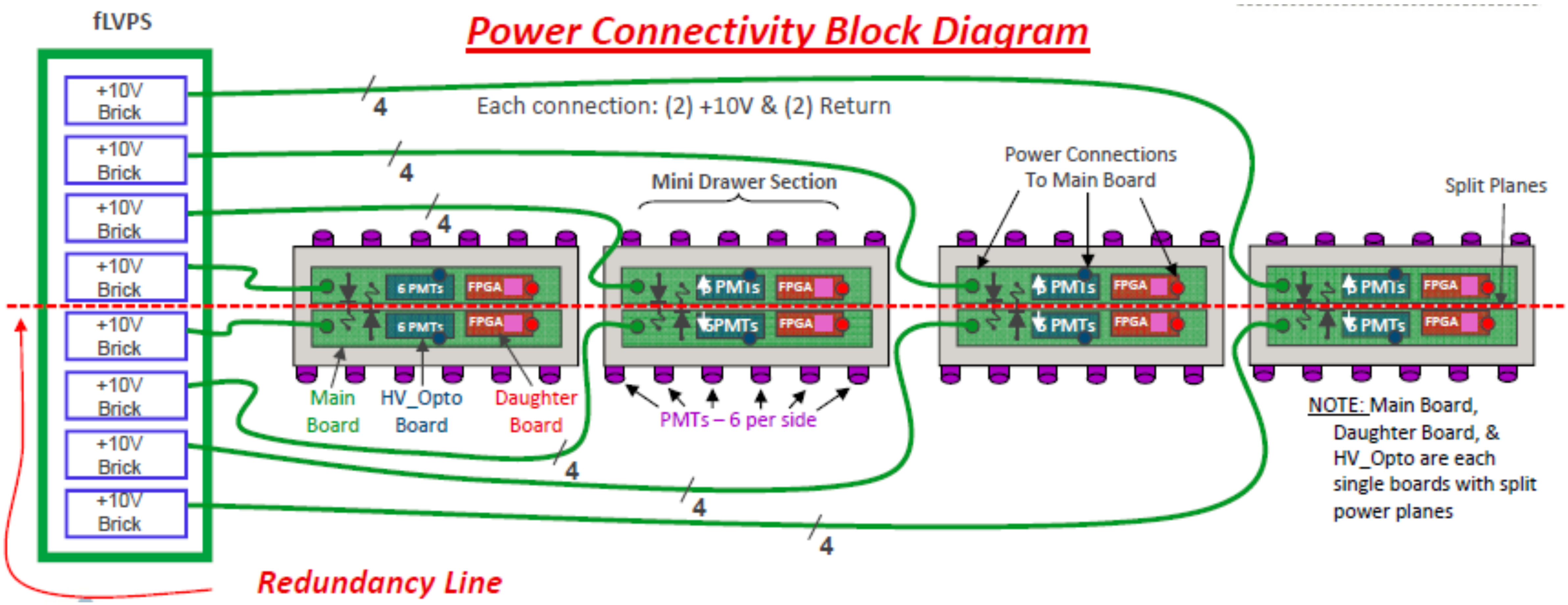


TilePPr production

Low voltage power supplies

- Moved to single 10 V feeder supplies; local point of load regulators on Main Board and Daughter Board
- High level of redundancy
- Evaluated during test beams

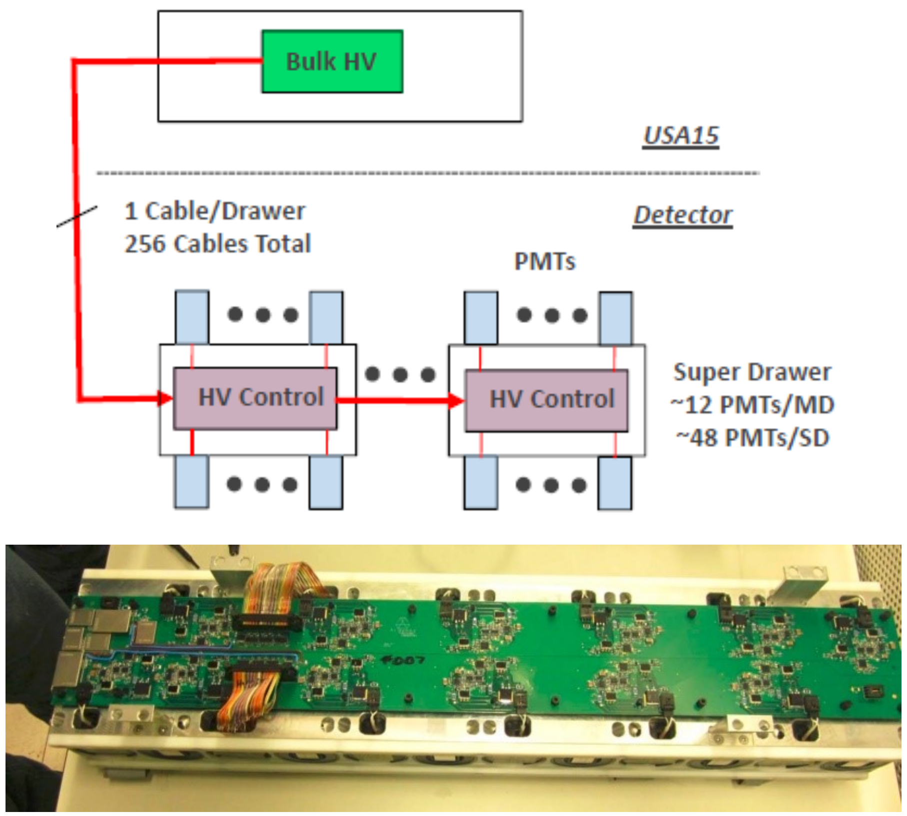




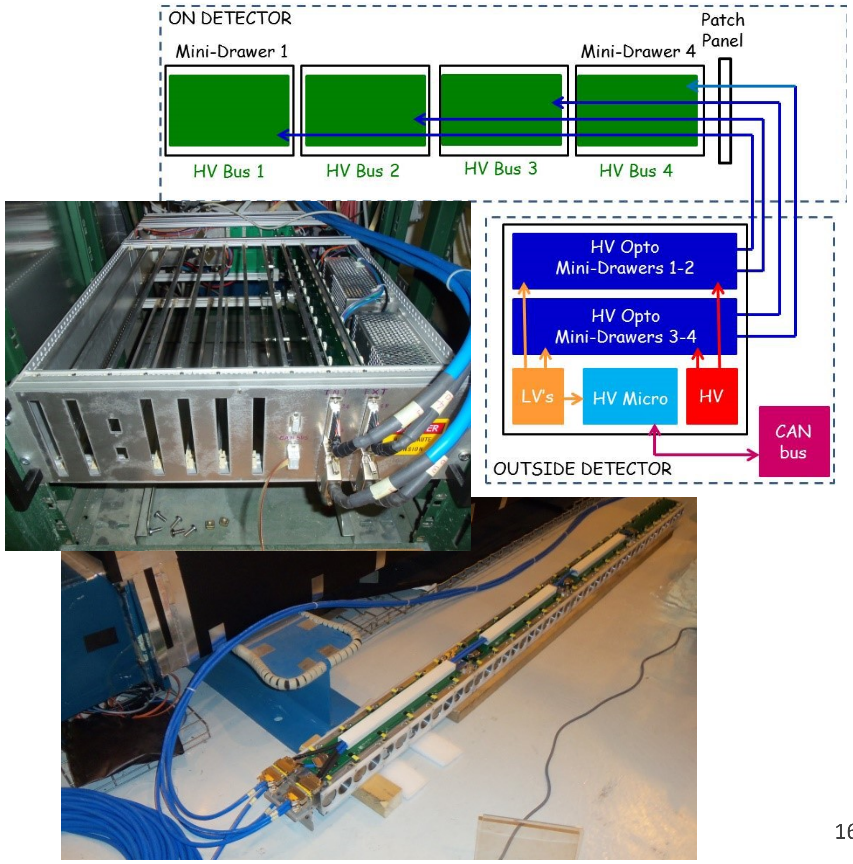
High voltage distribution systems

- Two options under consideration; local and remote high voltage
- The local system (HV_opto) uses existing cables to derive the voltages specific for each PMT on detector
  - A small number of channels are subject to ~1 SEU per year
- The remote system (HV_remote) is contingent on the availability of space for cables in the flexible chains
  - Baseline: Investigating having cables with 48 pairs in the Barrel and 32 pairs in the Extended Barrel (256 cables in total)
  - Radiation is not an issue

Local (HV_opto)

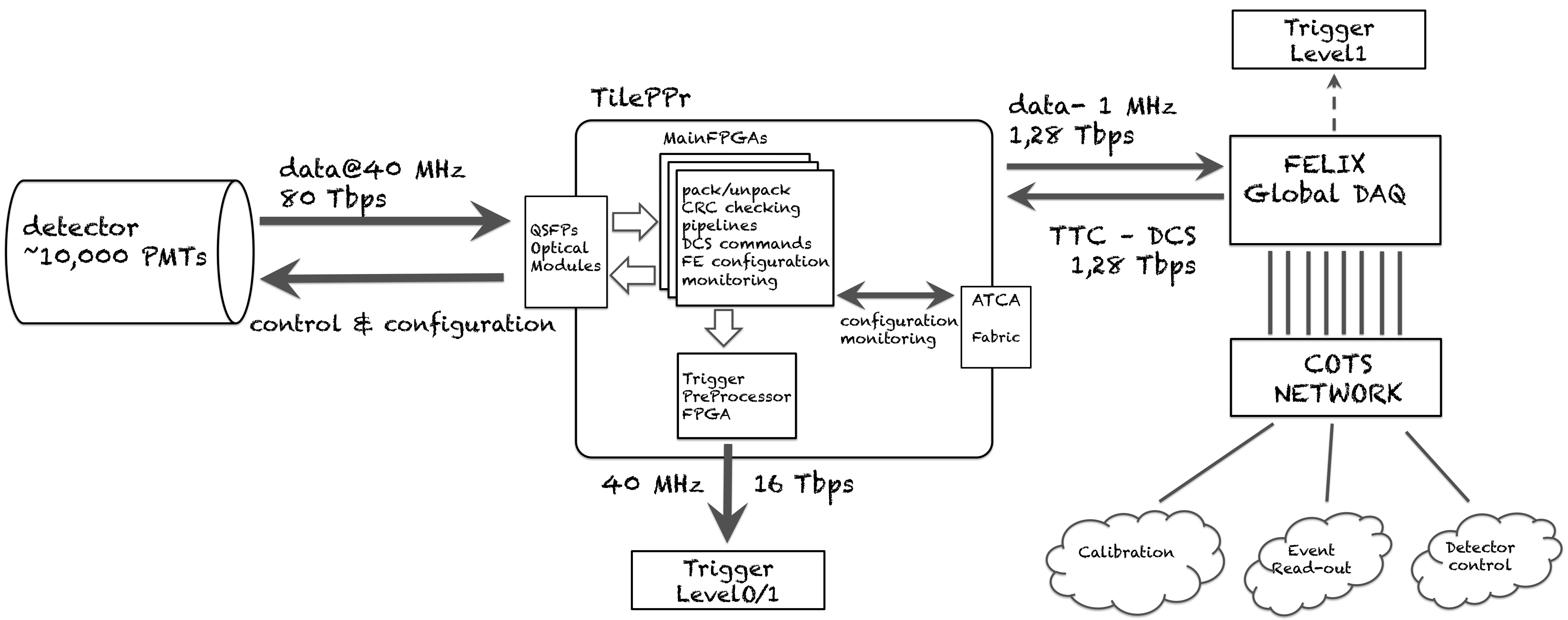


Remote (HV_remote)



Readout and trigger architecture

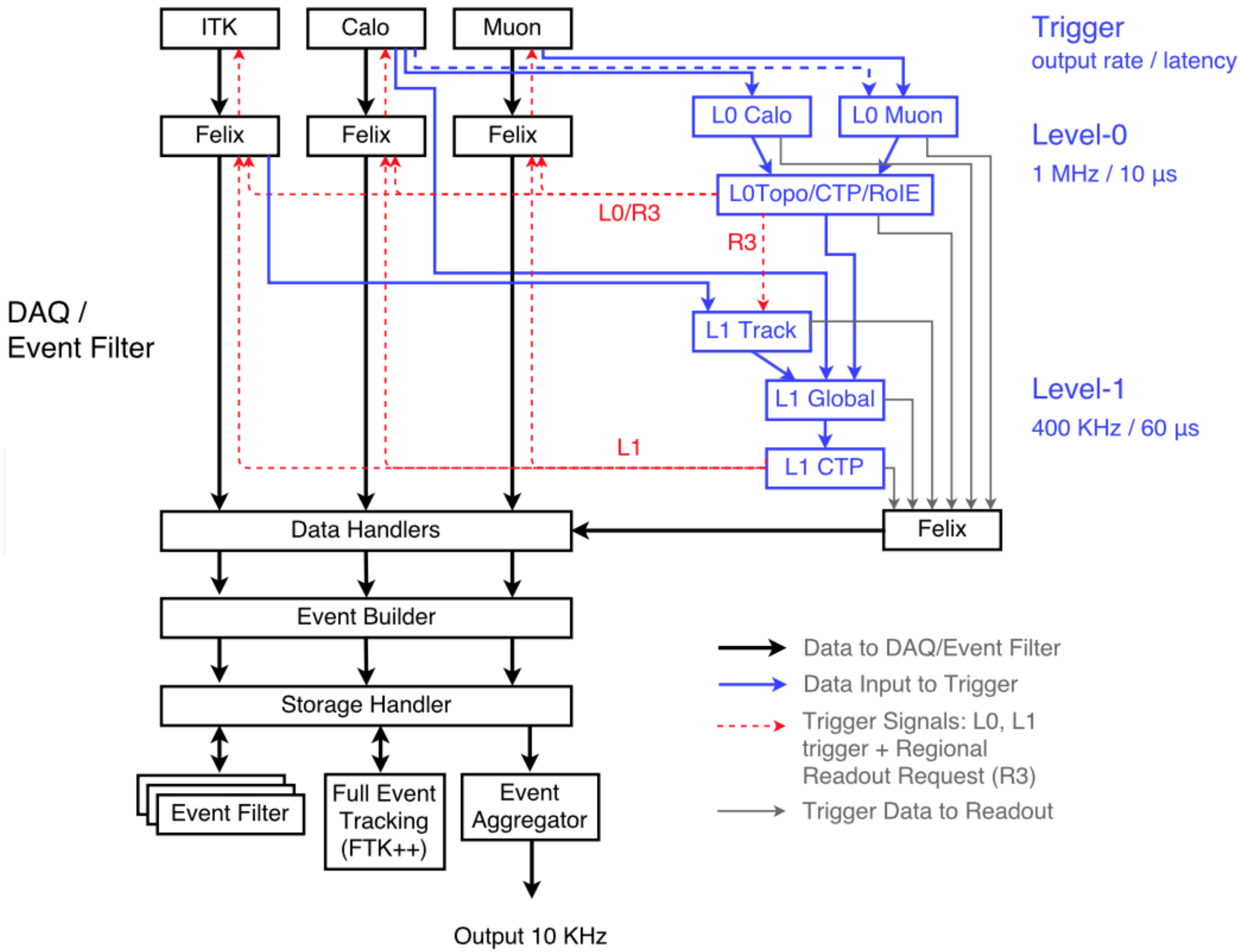
Source: [ATLAS-TILECAL-PROC-2015-025]



Readout and trigger architecture

Source: Tile Phase-II IDR

High-level description of the dual Level-0/Level-1 trigger system scheme (single level trigger system also under consideration)



Readout and trigger architecture

Source: Tile Phase-II IDR

Level-0 trigger rate	~1 MHz
Level-0 latency	~10 μs
Data rate to L0Calo and L0Muon	40 MHz
Latency data to L0Calo and L0Muon	~1.5 μs
Data rate to the FELIX	1 MHz-400 kHz
Latency data to FELIX	~60 μs

Table 1: Main trigger and readout parameters of the ATLAS Phase-II upgrade.

Up Link only	**Present**	**Upgrade**
Total Available Bandwidth	200 Gbps	80 Tbps
Number of fibers	256	8192
Fiber bandwidth	800 Mbps	9,6 Gbps
Number of modules	32	32
Number of crates	4 (VME)	4 (ATCA)
Input bandwidth per board	6,4 Gbps	2,5 Tbps
Out bandwidth to DAQ per module	3,2 Gbps	40 Gbps
Out bandwidth to trigger per module	Analog front-end	~500 Gbps

Table 2: The TileCal readout system in the present and Phase-II upgrade architectures. Bandwidth refer to available bandwidth in the link.